SSD1339

Advance Information

132RGB x 132 with 2 smart Icon lines Dot Matrix OLED/PLED Segment/Common Driver with Controller

SOLOMON SYSTECH

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TABLES

FIGURES

1 GERENAL DESCRIPTION

The SSD1339 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 396 segments (132RGB), 132 commons and 2 smart icon lines. This IC is designed for Common Cathode type OLED panel.

The SSD1339 displays data directly from its internal 132x133x18 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface. It has a 256 steps contrast control and 262k color control

2 FEATURES

- Support max. 132RGB x 132 matrix panel + icon line
- Power supply: V_{DD} = 2.4V ~ 3.5V
  V_{DDIO} = 1.5V ~ V_{DD}
  V_{CC} = 7.0V ~ 18.0V
- OLED driving output voltage: 16V maximum
- Segment maximum source current: 200uA
- Common maximum sink current: 80mA
- Embedded 132x133x18 bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Smart Icon mode
- Programmable color mode of 256, 65k, 262k
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- 8/9/16/18-bit 6800-series Parallel Interface, 8/9/16/18-bit 8080-series Parallel Interface and Serial Peripheral Interface.
- DC-DC voltage booster controller
- Wide range of operating temperature: -40 to 90 °C

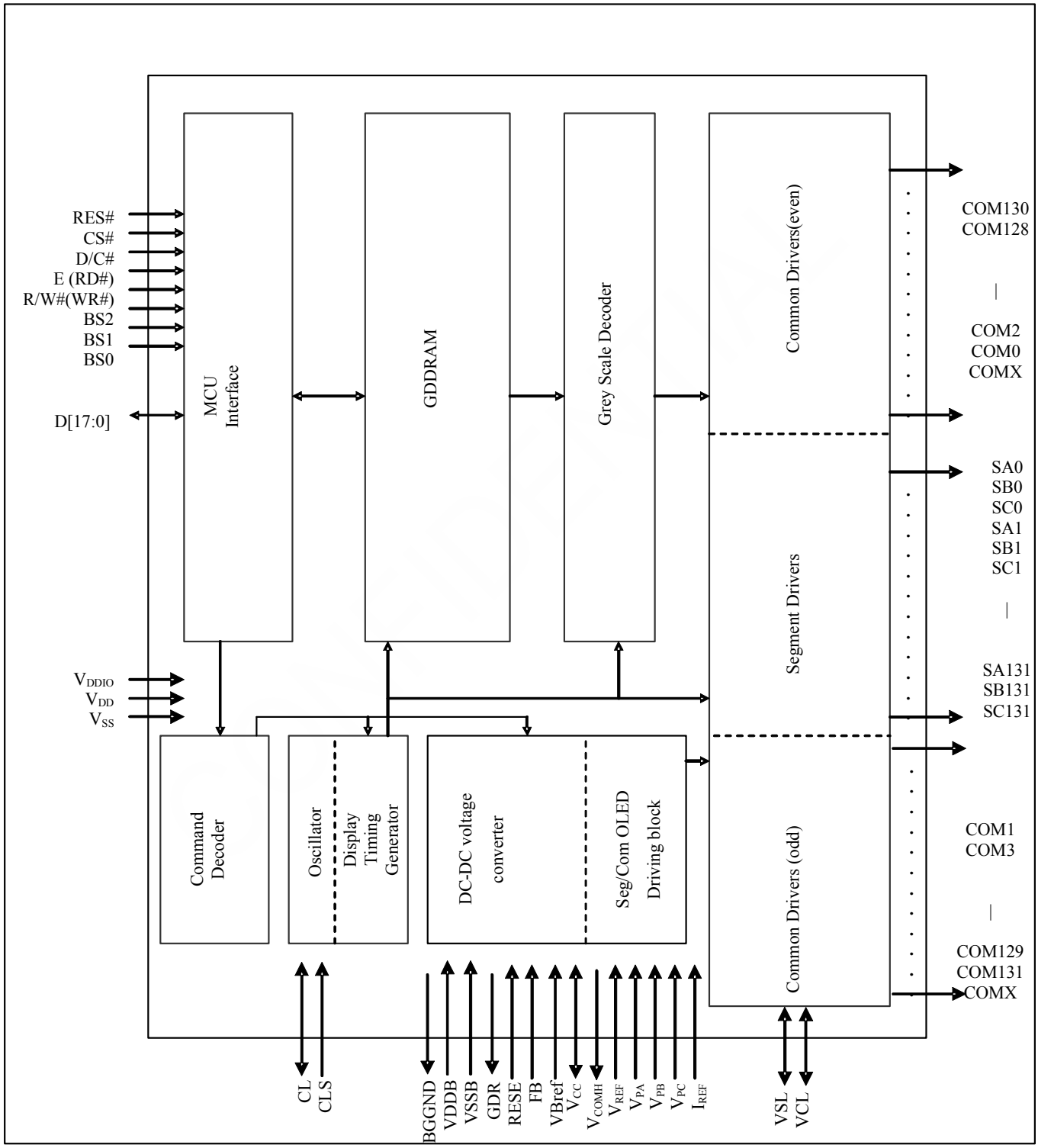
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1339Z	132RGB	132	COG	Page 10, 60	• Min SEG pad pitch: 41.2 um • Min COM pad pitch: 41.2 um
SSD1339U3R1	128RGB	128	COF	Page 16,61	• 48mm film • 80 / 68 / SPI interface • Output lead pitch: 0.0495mm for SEG 0.074925mm for COM • Reel form COF • 7 sprocket holes
SSD1339U3	128RGB	128	COF	Page 15, 64	• 80 / 68 / SPI interface • Output lead pitch: 0.0495mm for SEG 0.074925mm for COM • Punched COF with stiffener

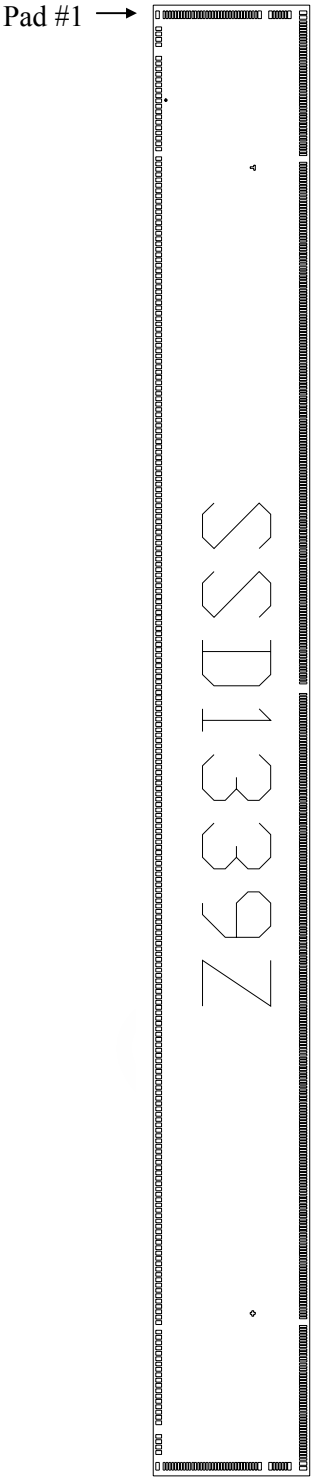
4 BLOCK DIAGRAM

Figure 4-1 : SSD1339 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1339Z pin assignment



+ represents the centre of the alignment mark

	X-pos (um)	Y-pos (um)
	-8176.0	307.0
	8176.0	307.0
	-9140.0	-941.0
	9140.0	-941.0

All alignment keys have size 75 um x 75 um

Die Size: 20989um x 2250um
Die Thickness: 457um +/- 25um
Min I/O pad pitch: 76.2 um
Min SEG pad pitch: 41.2 um
Min COM pad pitch: 41.2 um
Bump Height: Nominal 15 um

Table 5-1 : SSD1339Z Die Pad Coordinates

Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis
1	NC	-10160.275	-1043	81	TR0	-3886.2	-1043	161	VSS	2209.8	-1043
2	NC	-10084.075	-1043	82	VSS	-3810	-1043	162	R/W#(WR#)	2286	-1043
3	NC	-10007.875	-1043	83	VSSB	-3733.8	-1043	163	E(RD#)	2362.2	-1043
4	NC	-9931.675	-1043	84	VSSB	-3657.6	-1043	164	VDDIO	2438.4	-1043
5	NC	-9737.3	-1043	85	VSSB	-3581.4	-1043	165	D0	2514.6	-1043
6	NC	-9661.1	-1043	86	VSSB	-3505.2	-1043	166	D1	2590.8	-1043
7	NC	-9584.9	-1043	87	GDR	-3429	-1043	167	D2	2667	-1043
8	NC	-9508.7	-1043	88	GDR	-3352.8	-1043	168	D3	2743.2	-1043
9	NC	-9432.5	-1043	89	GDR	-3276.6	-1043	169	D4	2819.4	-1043
10	NC	-9356.3	-1043	90	GDR	-3200.4	-1043	170	D5	2895.6	-1043
11	NC	-9280.1	-1043	91	GDR	-3124.2	-1043	171	D6	2971.8	-1043
12	NC	-9203.9	-1043	92	GDR	-3048	-1043	172	D7	3048	-1043
13	NC	-9127.7	-1043	93	GDR	-2971.8	-1043	173	D8	3124.2	-1043
14	NC	-9051.5	-1043	94	GDR	-2895.6	-1043	174	D9	3200.4	-1043
15	NC	-8975.3	-1043	95	GDR	-2819.4	-1043	175	D10	3276.6	-1043
16	NC	-8899.1	-1043	96	GDR	-2743.2	-1043	176	D11	3352.8	-1043
17	NC	-8822.9	-1043	97	GDR	-2667	-1043	177	D12	3429	-1043
18	NC	-8746.7	-1043	98	GDR	-2590.8	-1043	178	D13	3505.2	-1043
19	NC	-8670.5	-1043	99	GDR	-2514.6	-1043	179	D14	3581.4	-1043
20	NC	-8594.3	-1043	100	GDR	-2438.4	-1043	180	D15	3657.6	-1043
21	NC	-8518.1	-1043	101	GDR	-2362.2	-1043	181	VDDIO	3733.8	-1043
22	NC	-8441.9	-1043	102	GDR	-2286	-1043	182	MS	3810	-1043
23	NC	-8305.8	-1043	103	GDR	-2209.8	-1043	183	CLS	3886.2	-1043
24	NC	-8229.6	-1043	104	GDR	-2133.6	-1043	184	D16	3962.4	-1043
25	NC	-8153.4	-1043	105	GDR	-2057.4	-1043	185	D17	4038.6	-1043
26	VCC	-8077.2	-1043	106	GDR	-1981.2	-1043	186	VSS	4114.8	-1043
27	VCC	-8001	-1043	107	VDDB	-1905	-1043	187	VSS	4191	-1043
28	VCC	-7924.8	-1043	108	VDDB	-1828.8	-1043	188	VSS	4267.2	-1043
29	VCC	-7848.6	-1043	109	VDDB	-1752.6	-1043	189	VSS	4343.4	-1043
30	VCC	-7772.4	-1043	110	VDDB	-1676.4	-1043	190	VSS	4419.6	-1043
31	VCC	-7696.2	-1043	111	VDD	-1600.2	-1043	191	VSS	4495.8	-1043
32	VCC	-7620	-1043	112	VDD	-1524	-1043	192	VCL	4572	-1043
33	VCC	-7543.8	-1043	113	VDD	-1447.8	-1043	193	VCL	4648.2	-1043
34	VCOMH	-7467.6	-1043	114	VDD	-1371.6	-1043	194	VCL	4724.4	-1043
35	VCOMH	-7391.4	-1043	115	FB	-1295.4	-1043	195	VCL	4800.6	-1043
36	VCOMH	-7315.2	-1043	116	VSS	-1219.2	-1043	196	VCL	4876.8	-1043
37	VSL	-7239	-1043	117	RESE	-1143	-1043	197	VCL	4953	-1043
38	VSL	-7162.8	-1043	118	VBREF	-1066.8	-1043	198	VCL	5029.2	-1043
39	VSL	-7086.6	-1043	119	VSS	-990.6	-1043	199	VCL	5105.4	-1043
40	VSL	-7010.4	-1043	120	BGGND	-914.4	-1043	200	VCL	5181.6	-1043
41	VSL	-6934.2	-1043	121	NC	-838.2	-1043	201	VCL	5257.8	-1043
42	VSL	-6858	-1043	122	VPA	-762	-1043	202	VCL	5334	-1043
43	VSL	-6781.8	-1043	123	VPB	-685.8	-1043	203	VCL	5410.2	-1043
44	VSL	-6705.6	-1043	124	VPC	-609.6	-1043	204	VDD	5486.4	-1043
45	VSL	-6629.4	-1043	125	VSS	-533.4	-1043	205	VDD	5562.6	-1043
46	VDD	-6553.2	-1043	126	NC	-457.2	-1043	206	VDD	5638.8	-1043
47	VDD	-6477	-1043	127	VSS	-381	-1043	207	VDD	5715	-1043
48	VDD	-6400.8	-1043	128	GPIO0	-304.8	-1043	208	VDD	5791.2	-1043
49	VDD	-6324.6	-1043	129	GPIO1	-228.6	-1043	209	VDD	5867.4	-1043
50	VDD	-6248.4	-1043	130	VDDIO	-152.4	-1043	210	VDD	5943.6	-1043
51	VDD	-6172.2	-1043	131	ICASC	-76.2	-1043	211	VDD	6019.8	-1043
52	VDD	-6096	-1043	132	ICASB	0	-1043	212	VSL	6096	-1043
53	VDD	-6019.8	-1043	133	ICASA	76.2	-1043	213	VSL	6172.2	-1043
54	VCL	-5943.6	-1043	134	VSS	152.4	-1043	214	VSL	6248.4	-1043
55	VCL	-5867.4	-1043	135	VREF	228.6	-1043	215	VSL	6324.6	-1043
56	VCL	-5791.2	-1043	136	VCC	304.8	-1043	216	VSL	6400.8	-1043
57	VCL	-5715	-1043	137	VMONA	381	-1043	217	VSL	6477	-1043
58	VCL	-5638.8	-1043	138	VMONA	457.2	-1043	218	VSL	6553.2	-1043
59	VCL	-5562.6	-1043	139	VCC	533.4	-1043	219	VSL	6629.4	-1043
60	VCL	-5486.4	-1043	140	VCC	609.6	-1043	220	VSL	6705.6	-1043
61	VCL	-5410.2	-1043	141	VCC	685.8	-1043	221	VSL	6781.8	-1043
62	VCL	-5334	-1043	142	VCC	762	-1043	222	VSL	6858	-1043
63	VSS	-5257.8	-1043	143	VCC	838.2	-1043	223	VSL	6934.2	-1043
64	VSS	-5181.6	-1043	144	VSS	914.4	-1043	224	VDDIO	7010.4	-1043
65	VSS	-5105.4	-1043	145	IREF	990.6	-1043	225	VDDIO	7086.6	-1043
66	VSS	-5029.2	-1043	146	M	1066.8	-1043	226	VCOMH	7162.8	-1043
67	VSS	-4953	-1043	147	CL	1143	-1043	227	VCOMH	7239	-1043
68	VSS	-4876.8	-1043	148	DOF#	1219.2	-1043	228	VCOMH	7315.2	-1043
69	VSSB	-4800.6	-1043	149	RES#	1295.4	-1043	229	VCOMH	7391.4	-1043
70	VSSB	-4724.4	-1043	150	VSS	1371.6	-1043	230	VCOMH	7467.6	-1043
71	VSSB	-4648.2	-1043	151	D/C#	1447.8	-1043	231	VCC	7543.8	-1043
72	VSSB	-4572	-1043	152	VDDIO	1524	-1043	232	VCC	7620	-1043
73	TR8	-4495.8	-1043	153	CS#	1600.2	-1043	233	VCC	7696.2	-1043
74	TR7	-4419.6	-1043	154	VSS	1676.4	-1043	234	VCC	7772.4	-1043
75	TR6	-4343.4	-1043	155	BS2	1752.6	-1043	235	VCC	7848.6	-1043
76	TR5	-4267.2	-1043	156	VDDIO	1828.8	-1043	236	VCC	7924.8	-1043
77	TR4	-4191	-1043	157	BS1	1905	-1043	237	VCC	8001	-1043
78	TR3	-4114.8	-1043	158	VSS	1981.2	-1043	238	VCC	8077.2	-1043
79	TR2	-4038.6	-1043	159	BS0	2057.4	-1043	239	NC	8153.4	-1043
80	TR1	-3962.4	-1043	160	VDDIO	2133.6	-1043	240	NC	8229.6	-1043

Pad #	Pad Name	X-Axis	Y-Axis
241	NC	8305.8	-1043
242	NC	8441.9	-1043
243	NC	8518.1	-1043
244	NC	8594.3	-1043
245	NC	8670.5	-1043
246	NC	8746.7	-1043
247	NC	8822.9	-1043
248	NC	8899.1	-1043
249	NC	8975.3	-1043
250	NC	9051.5	-1043
251	NC	9127.7	-1043
252	NC	9203.9	-1043
253	NC	9280.1	-1043
254	NC	9356.3	-1043
255	NC	9432.5	-1043
256	NC	9508.7	-1043
257	NC	9584.9	-1043
258	NC	9661.1	-1043
259	NC	9737.3	-1043
260	NC	9931.675	-1043
261	NC	10007.875	-1043
262	NC	10084.075	-1043
263	NC	10160.275	-1043
264	NC	10359.7	-1060
265	COM65	10359.7	-967
266	COM64	10359.7	-925.8
267	COM63	10359.7	-884.6
268	COM62	10359.7	-843.4
269	COM61	10359.7	-802.2
270	COM60	10359.7	-761
271	COM59	10359.7	-719.8
272	COM58	10359.7	-678.6
273	COM57	10359.7	-637.4
274	COM56	10359.7	-596.2
275	COM55	10359.7	-555
276	COM54	10359.7	-513.8
277	COM53	10359.7	-472.6
278	COM52	10359.7	-431.4
279	COM51	10359.7	-390.2
280	COM50	10359.7	-349
281	COM49	10359.7	-307.8
282	COM48	10359.7	-266.6
283	COM47	10359.7	-225.4
284	COM46	10359.7	-184.2
285	COM45	10359.7	-143
286	COM44	10359.7	-101.8
287	NC	10359.7	-60.6
288	NC	10359.7	-19.4
289	NC	10359.7	21.8
290	NC	10359.7	63
291	NC	10359.7	104.2
292	NC	10359.7	145.4
293	NC	10359.7	186.6
294	NC	10359.7	227.8
295	NC	10359.7	269
296	NC	10359.7	310.2
297	NC	10359.7	351.4
298	NC	10359.7	404.1
299	NC	10359.7	562.95
300	NC	10359.7	615.65
301	NC	10359.7	656.85
302	NC	10359.7	698.05
303	NC	10359.7	739.25
304	NC	10359.7	780.45
305	NC	10359.7	833.15
306	NC	10389.7	1030
307	NC	10318.5	1030
308	COM43	10258.8	1030
309	COM42	10217.6	1030
310	COM41	10176.4	1030
311	COM40	10135.2	1030
312	COM39	10094	1030
313	COM38	10052.8	1030
314	COM37	10011.6	1030
315	COM36	9970.4	1030
316	COM35	9929.2	1030
317	COM34	9888	1030
318	COM33	9846.8	1030
319	COM32	9805.6	1030
320	COM31	9764.4	1030
321	COM30	9723.2	1030
322	COM29	9682	1030
323	COM28	9640.8	1030
324	COM27	9599.6	1030
325	COM26	9558.4	1030
326	COM25	9517.2	1030
327	COM24	9476	1030
328	COM23	9434.8	1030
329	COM22	9393.6	1030
330	COM21	9352.4	1030
331	COM20	9311.2	1030
332	COM19	9270	1030
333	COM18	9228.8	1030
334	COM17	9187.6	1030
335	COM16	9146.4	1030
336	COM15	9105.2	1030
337	COM14	9064	1030
338	COM13	9022.8	1030
339	COM12	8981.6	1030
340	COM11	8940.4	1030
341	COM10	8899.2	1030
342	COM9	8858	1030
343	COM8	8816.8	1030
344	COM7	8775.6	1030
345	COM6	8734.4	1030
346	COM5	8693.2	1030
347	COM4	8652	1030
348	COM3	8610.8	1030
349	COM2	8569.6	1030
350	COM1	8528.4	1030
351	COM0	8487.2	1030
352	COMX	8446	1030
353	NC	8404.8	1030
354	NC	8363.6	1030
355	NC	8240	1030
356	SA0	8198.8	1030
357	SB0	8157.6	1030
358	SC0	8116.4	1030
359	SA1	8075.2	1030
360	SB1	8034	1030
361	SC1	7992.8	1030
362	SA2	7951.6	1030
363	SB2	7910.4	1030
364	SC2	7869.2	1030
365	SA3	7828	1030
366	SB3	7786.8	1030
367	SC3	7745.6	1030
368	SA4	7704.4	1030
369	SB4	7663.2	1030
370	SC4	7622	1030
371	SA5	7580.8	1030
372	SB5	7539.6	1030
373	SC5	7498.4	1030
374	SA6	7457.2	1030
375	SB6	7416	1030
376	SC6	7374.8	1030
377	SA7	7333.6	1030
378	SB7	7292.4	1030
379	SC7	7251.2	1030
380	SA8	7210	1030
381	SB8	7168.8	1030
382	SC8	7127.6	1030
383	SA9	7086.4	1030
384	SB9	7045.2	1030
385	SC9	7004	1030
386	SA10	6962.8	1030
387	SB10	6921.6	1030
388	SC10	6880.4	1030
389	SA11	6839.2	1030
390	SB11	6798	1030
391	SC11	6756.8	1030
392	SA12	6715.6	1030
393	SB12	6674.4	1030
394	SC12	6633.2	1030
395	SA13	6592	1030
396	SB13	6550.8	1030
397	SC13	6509.6	1030
398	SA14	6468.4	1030
399	SB14	6427.2	1030
400	SC14	6386	1030
401	SA15	6344.8	1030
402	SB15	6303.6	1030
403	SC15	6262.4	1030
404	SA16	6221.2	1030
405	SB16	6180	1030
406	SC16	6138.8	1030
407	SA17	6097.6	1030
408	SB17	6056.4	1030
409	SC17	6015.2	1030
410	SA18	5974	1030
411	SB18	5932.8	1030
412	SC18	5891.6	1030
413	SA19	5850.4	1030
414	SB19	5809.2	1030
415	SC19	5768	1030
416	SA20	5726.8	1030
417	SB20	5685.6	1030
418	SC20	5644.4	1030
419	SA21	5603.2	1030
420	SB21	5562	1030
421	SC21	5520.8	1030
422	SA22	5479.6	1030
423	SB22	5438.4	1030
424	SC22	5397.2	1030
425	SA23	5356	1030
426	SB23	5314.8	1030
427	SC23	5273.6	1030
428	SA24	5232.4	1030
429	SB24	5191.2	1030
430	SC24	5150	1030
431	SA25	5108.8	1030
432	SB25	5067.6	1030
433	SC25	5026.4	1030
434	SA26	4985.2	1030
435	SB26	4944	1030
436	SC26	4902.8	1030
437	SA27	4861.6	1030
438	SB27	4820.4	1030
439	SC27	4779.2	1030
440	SA28	4738	1030
441	SB28	4696.8	1030
442	SC28	4655.6	1030
443	SA29	4614.4	1030
444	SB29	4573.2	1030
445	SC29	4532	1030
446	SA30	4490.8	1030
447	SB30	4449.6	1030
448	SC30	4408.4	1030
449	SA31	4367.2	1030
450	SB31	4326	1030
451	SC31	4284.8	1030
452	SA32	4243.6	1030
453	SB32	4202.4	1030
454	SC32	4161.2	1030
455	SA33	4120	1030
456	SB33	4078.8	1030
457	SC33	4037.6	1030
458	SA34	3996.4	1030
459	SB34	3955.2	1030
460	SC34	3914	1030
461	SA35	3872.8	1030
462	SB35	3831.6	1030
463	SC35	3790.4	1030
464	SA36	3749.2	1030
465	SB36	3708	1030
466	SC36	3666.8	1030
467	SA37	3625.6	1030
468	SB37	3584.4	1030
469	SC37	3543.2	1030
470	SA38	3502	1030
471	SB38	3460.8	1030
472	SC38	3419.6	1030
473	SA39	3378.4	1030
474	SB39	3337.2	1030
475	SC39	3296	1030
476	SA40	3254.8	1030
477	SB40	3213.6	1030
478	SC40	3172.4	1030
479	SA41	3131.2	1030
480	SB41	3090	1030

Pad #	Pad Name	X-Axis	Y-Axis
481	SC41	3048.8	1030
482	SA42	3007.6	1030
483	SB42	2966.4	1030
484	SC42	2925.2	1030
485	SA43	2884	1030
486	SB43	2842.8	1030
487	SC43	2801.6	1030
488	SA44	2760.4	1030
489	SB44	2719.2	1030
490	SC44	2678	1030
491	SA45	2636.8	1030
492	SB45	2595.6	1030
493	SC45	2554.4	1030
494	SA46	2513.2	1030
495	SB46	2472	1030
496	SC46	2430.8	1030
497	SA47	2389.6	1030
498	SB47	2348.4	1030
499	SC47	2307.2	1030
500	SA48	2266	1030
501	SB48	2224.8	1030
502	SC48	2183.6	1030
503	SA49	2142.4	1030
504	SB49	2101.2	1030
505	SC49	2060	1030
506	SA50	2018.8	1030
507	SB50	1977.6	1030
508	SC50	1936.4	1030
509	SA51	1895.2	1030
510	SB51	1854	1030
511	SC51	1812.8	1030
512	SA52	1771.6	1030
513	SB52	1730.4	1030
514	SC52	1689.2	1030
515	SA53	1648	1030
516	SB53	1606.8	1030
517	SC53	1565.6	1030
518	SA54	1524.4	1030
519	SB54	1483.2	1030
520	SC54	1442	1030
521	SA55	1400.8	1030
522	SB55	1359.6	1030
523	SC55	1318.4	1030
524	SA56	1277.2	1030
525	SB56	1236	1030
526	SC56	1194.8	1030
527	SA57	1153.6	1030
528	SB57	1112.4	1030
529	SC57	1071.2	1030
530	SA58	1030	1030
531	SB58	988.8	1030
532	SC58	947.6	1030
533	SA59	906.4	1030
534	SB59	865.2	1030
535	SC59	824	1030
536	SA60	782.8	1030
537	SB60	741.6	1030
538	SC60	700.4	1030
539	SA61	659.2	1030
540	SB61	618	1030
541	SC61	576.8	1030
542	SA62	535.6	1030
543	SB62	494.4	1030
544	SC62	453.2	1030
545	SA63	412	1030
546	SB63	370.8	1030
547	SC63	329.6	1030
548	SA64	288.4	1030
549	SB64	247.2	1030
550	SC64	206	1030
551	SA65	164.8	1030
552	SB65	123.6	1030
553	SC65	82.4	1030
554	SA66	41.2	1030
555	SB66	0	1030
556	SC66	-41.2	1030
557	SA67	-82.4	1030
558	SB67	-123.6	1030
559	SC67	-164.8	1030
560	SA68	-206	1030
561	SB68	-247.2	1030
562	SC68	-288.4	1030
563	SA69	-329.6	1030
564	SB69	-370.8	1030
565	SC69	-412	1030
566	SA70	-453.2	1030
567	SB70	-494.4	1030
568	SC70	-535.6	1030
569	SA71	-576.8	1030
570	SB71	-618	1030
571	SC71	-659.2	1030
572	SA72	-824	1030
573	SB72	-865.2	1030
574	SC72	-906.4	1030
575	SA73	-947.6	1030
576	SB73	-988.8	1030
577	SC73	-1030	1030
578	SA74	-1071.2	1030
579	SB74	-1112.4	1030
580	SC74	-1153.6	1030
581	SA75	-1194.8	1030
582	SB75	-1236	1030
583	SC75	-1277.2	1030
584	SA76	-1318.4	1030
585	SB76	-1359.6	1030
586	SC76	-1400.8	1030
587	SA77	-1442	1030
588	SB77	-1483.2	1030
589	SC77	-1524.4	1030
590	SA78	-1565.6	1030
591	SB78	-1606.8	1030
592	SC78	-1648	1030
593	SA79	-1689.2	1030
594	SB79	-1730.4	1030
595	SC79	-1771.6	1030
596	SA80	-1812.8	1030
597	SB80	-1854	1030
598	SC80	-1895.2	1030
599	SA81	-1936.4	1030
600	SB81	-1977.6	1030
601	SC81	-2018.8	1030
602	SA82	-2060	1030
603	SB82	-2101.2	1030
604	SC82	-2142.4	1030
605	SA83	-2183.6	1030
606	SB83	-2224.8	1030
607	SC83	-2266	1030
608	SA84	-2307.2	1030
609	SB84	-2348.4	1030
610	SC84	-2389.6	1030
611	SA85	-2430.8	1030
612	SB85	-2472	1030
613	SC85	-2513.2	1030
614	SA86	-2554.4	1030
615	SB86	-2595.6	1030
616	SC86	-2636.8	1030
617	SA87	-2678	1030
618	SB87	-2719.2	1030
619	SC87	-2760.4	1030
620	SA88	-2801.6	1030
621	SB88	-2842.8	1030
622	SC88	-2884	1030
623	SA89	-2925.2	1030
624	SB89	-2966.4	1030
625	SC89	-3007.6	1030
626	SA90	-3048.8	1030
627	SB90	-3090	1030
628	SC90	-3131.2	1030
629	SA91	-3172.4	1030
630	SB91	-3213.6	1030
631	SC91	-3254.8	1030
632	SA92	-3296	1030
633	SB92	-3337.2	1030
634	SC92	-3378.4	1030
635	SA93	-3419.6	1030
636	SB93	-3460.8	1030
637	SC93	-3502	1030
638	SA94	-3543.2	1030
639	SB94	-3584.4	1030
640	SC94	-3625.6	1030
641	SA95	-3666.8	1030
642	SB95	-3708	1030
643	SC95	-3749.2	1030
644	SA96	-3790.4	1030
645	SB96	-3831.6	1030
646	SC96	-3872.8	1030
647	SA97	-3914	1030
648	SB97	-3955.2	1030
649	SC97	-3996.4	1030
650	SA98	-4037.6	1030
651	SB98	-4078.8	1030
652	SC98	-4120	1030
653	SA99	-4161.2	1030
654	SB99	-4202.4	1030
655	SC99	-4243.6	1030
656	SA100	-4284.8	1030
657	SB100	-4326	1030
658	SC100	-4367.2	1030
659	SA101	-4408.4	1030
660	SB101	-4449.6	1030
661	SC101	-4490.8	1030
662	SA102	-4532	1030
663	SB102	-4573.2	1030
664	SC102	-4614.4	1030
665	SA103	-4655.6	1030
666	SB103	-4696.8	1030
667	SC103	-4738	1030
668	SA104	-4779.2	1030
669	SB104	-4820.4	1030
670	SC104	-4861.6	1030
671	SA105	-4902.8	1030
672	SB105	-4944	1030
673	SC105	-4985.2	1030
674	SA106	-5026.4	1030
675	SB106	-5067.6	1030
676	SC106	-5108.8	1030
677	SA107	-5150	1030
678	SB107	-5191.2	1030
679	SC107	-5232.4	1030
680	SA108	-5273.6	1030
681	SB108	-5314.8	1030
682	SC108	-5356	1030
683	SA109	-5397.2	1030
684	SB109	-5438.4	1030
685	SC109	-5479.6	1030
686	SA110	-5520.8	1030
687	SB110	-5562	1030
688	SC110	-5603.2	1030
689	SA111	-5644.4	1030
690	SB111	-5685.6	1030
691	SC111	-5726.8	1030
692	SA112	-5768	1030
693	SB112	-5809.2	1030
694	SC112	-5850.4	1030
695	SA113	-5891.6	1030
696	SB113	-5932.8	1030
697	SC113	-5974	1030
698	SA114	-6015.2	1030
699	SB114	-6056.4	1030
700	SC114	-6097.6	1030
701	SA115	-6138.8	1030
702	SB115	-6180	1030
703	SC115	-6221.2	1030
704	SA116	-6262.4	1030
705	SB116	-6303.6	1030
706	SC116	-6344.8	1030
707	SA117	-6386	1030
708	SB117	-6427.2	1030
709	SC117	-6468.4	1030
710	SA118	-6509.6	1030
711	SB118	-6550.8	1030
712	SC118	-6592	1030
713	SA119	-6633.2	1030
714	SB119	-6674.4	1030
715	SC119	-6715.6	1030
716	SA120	-6756.8	1030
717	SB120	-6798	1030
718	SC120	-6839.2	1030
719	SA121	-6880.4	1030
720	SB121	-6921.6	1030

Pad #	Pad Name	X-Axis	Y-Axis
721	SC121	-6962.8	1030
722	SA122	-7004	1030
723	SB122	-7045.2	1030
724	SC122	-7086.4	1030
725	SA123	-7127.6	1030
726	SB123	-7168.8	1030
727	SC123	-7210	1030
728	SA124	-7251.2	1030
729	SB124	-7292.4	1030
730	SC124	-7333.6	1030
731	SA125	-7374.8	1030
732	SB125	-7416	1030
733	SC125	-7457.2	1030
734	SA126	-7498.4	1030
735	SB126	-7539.6	1030
736	SC126	-7580.8	1030
737	SA127	-7622	1030
738	SB127	-7663.2	1030
739	SC127	-7704.4	1030
740	SA128	-7745.6	1030
741	SB128	-7786.8	1030
742	SC128	-7828	1030
743	SA129	-7869.2	1030
744	SB129	-7910.4	1030
745	SC129	-7951.6	1030
746	SA130	-7992.8	1030
747	SB130	-8034	1030
748	SC130	-8075.2	1030
749	SA131	-8116.4	1030
750	SB131	-8157.6	1030
751	SC131	-8198.8	1030
752	NC	-8240	1030
753	NC	-8363.6	1030
754	NC	-8404.8	1030
755	COM66	-8446	1030
756	COM67	-8487.2	1030
757	COM68	-8528.4	1030
758	COM69	-8569.6	1030
759	COM70	-8610.8	1030
760	COM71	-8652	1030
761	COM72	-8693.2	1030
762	COM73	-8734.4	1030
763	COM74	-8775.6	1030
764	COM75	-8816.8	1030
765	COM76	-8858	1030
766	COM77	-8899.2	1030
767	COM78	-8940.4	1030
768	COM79	-8981.6	1030
769	COM80	-9022.8	1030
770	COM81	-9064	1030
771	COM82	-9105.2	1030
772	COM83	-9146.4	1030
773	COM84	-9187.6	1030
774	COM85	-9228.8	1030
775	COM86	-9270	1030
776	COM87	-9311.2	1030
777	COM88	-9352.4	1030
778	COM89	-9393.6	1030
779	COM90	-9434.8	1030
780	COM91	-9476	1030
781	COM92	-9517.2	1030
782	COM93	-9558.4	1030
783	COM94	-9599.6	1030
784	COM95	-9640.8	1030
785	COM96	-9682	1030
786	COM97	-9723.2	1030
787	COM98	-9764.4	1030
788	COM99	-9805.6	1030
789	COM100	-9846.8	1030
790	COM101	-9888	1030
791	COM102	-9929.2	1030
792	COM103	-9970.4	1030
793	COM104	-10011.6	1030
794	COM105	-10052.8	1030
795	COM106	-10094	1030
796	COM107	-10135.2	1030
797	COM108	-10176.4	1030
798	COM109	-10217.6	1030
799	COM110	-10258.8	1030
800	NC	-10318.5	1030

Pad #	Pad Name	X-Axis	Y-Axis
801	NC	-10389.7	1030
802	NC	-10359.7	833.15
803	NC	-10359.7	780.45
804	NC	-10359.7	739.25
805	NC	-10359.7	698.05
806	NC	-10359.7	656.85
807	NC	-10359.7	615.65
808	NC	-10359.7	562.95
809	NC	-10359.7	404.1
810	NC	-10359.7	351.4
811	NC	-10359.7	310.2
812	NC	-10359.7	269
813	NC	-10359.7	227.8
814	NC	-10359.7	186.6
815	NC	-10359.7	145.4
816	NC	-10359.7	104.2
817	NC	-10359.7	63
818	NC	-10359.7	21.8
819	NC	-10359.7	-19.4
820	NC	-10359.7	-60.6
821	COM111	-10359.7	-101.8
822	COM112	-10359.7	-143
823	COM113	-10359.7	-184.2
824	COM114	-10359.7	-225.4
825	COM115	-10359.7	-266.6
826	COM116	-10359.7	-307.8
827	COM117	-10359.7	-349
828	COM118	-10359.7	-390.2
829	COM119	-10359.7	-431.4
830	COM120	-10359.7	-472.6
831	COM121	-10359.7	-513.8
832	COM122	-10359.7	-555
833	COM123	-10359.7	-596.2
834	COM124	-10359.7	-637.4
835	COM125	-10359.7	-678.6
836	COM126	-10359.7	-719.8
837	COM127	-10359.7	-761
838	COM128	-10359.7	-802.2
839	COM129	-10359.7	-843.4
840	COM130	-10359.7	-884.6
841	COM131	-10359.7	-925.8
842	COMX	-10359.7	-967
843	NC	-10359.7	-1060

Die Size: **20989um x 2250um**

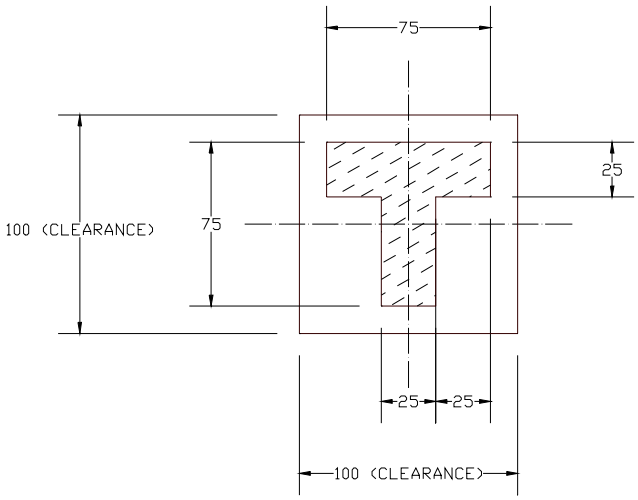
Gold Bump Face Up

Pad 1, 2 ,3, … -->

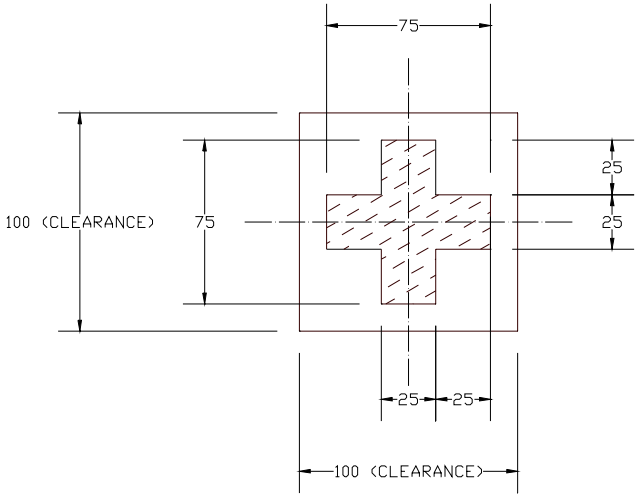
Pad #	X-Dimension	Y-Dimension
1 - 263	54um	84um
264, 298-299, 305, 802, 808-809, 843	110um	50um
265-297, 300-304, 803-807, 810-842	110um	27um
306-307, 800-801	50um	110um
308-799	27um	110um

Marks	X-Axis	Y-Axis
KEY_O	9140.000	-941.000
KEY_O	-9140.000	-941.000
KEY_T	-8176.000	307.000
KEY_X	8176.000	307.000

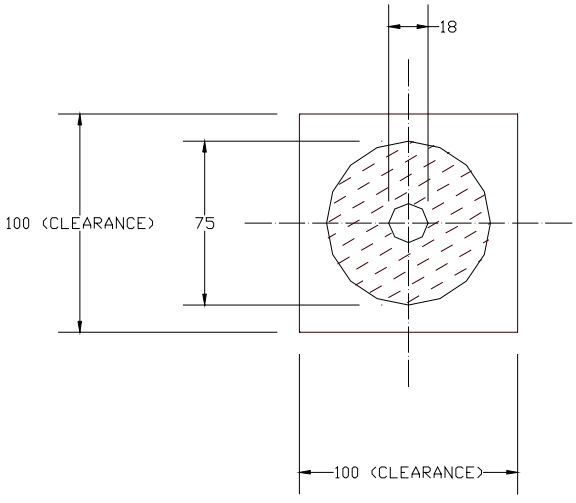
Figure 5-2 : SSD1339Z alignment mark dimensions



T shape



+ shape



Circle

*All units are in um

6 PIN ARRANGEMENT

6.1 SSD1339U3R1 Pin Assignment

Figure 6-1 : SSD1339U3R1 pin assignment

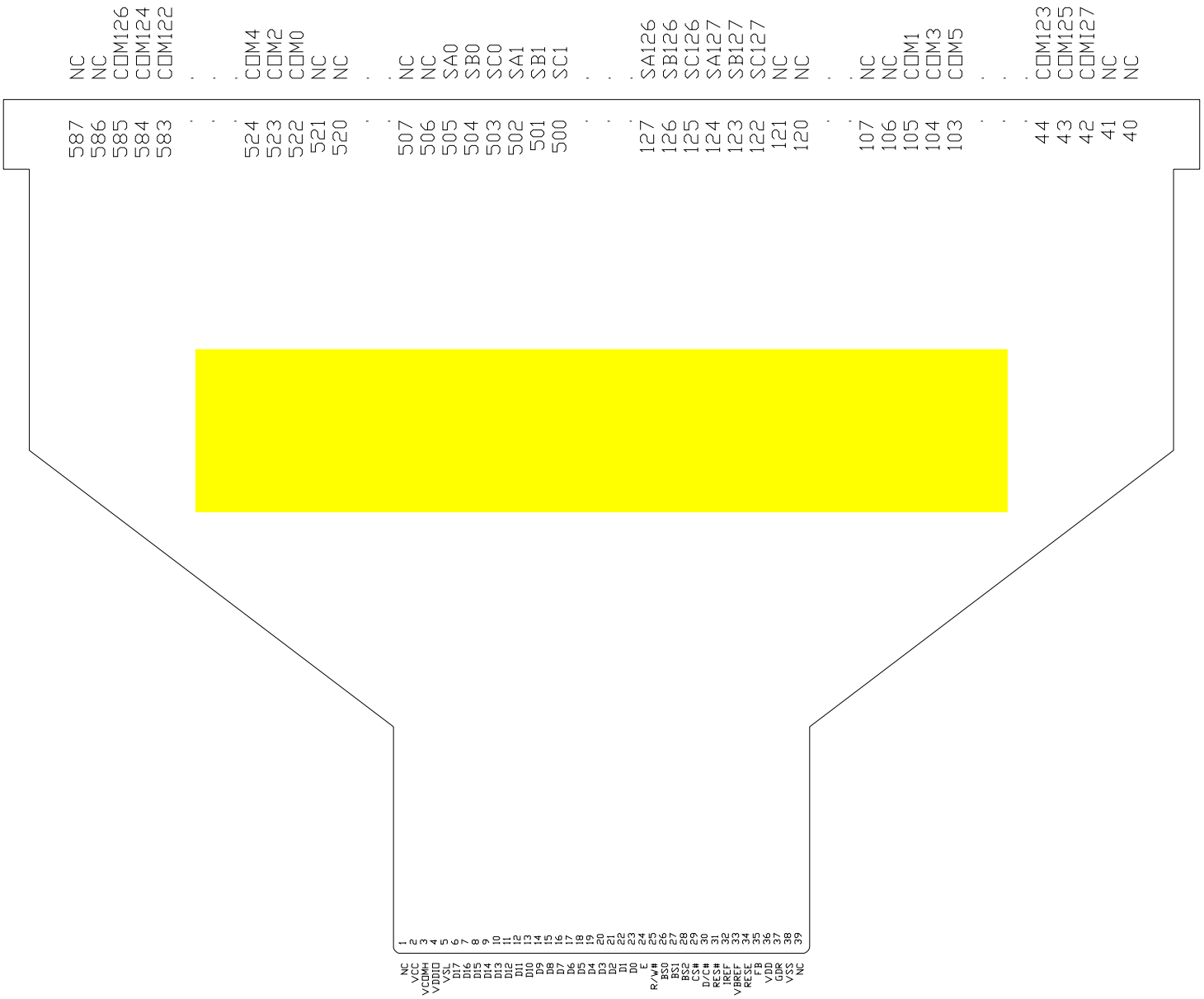


Table 6-1 - SSD1339U3R1 pin assignment

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
NC	1	COM49	81	SC114	161	SA88	241	SB61	321	SC34	401	SA8	481	COM78	561
VCC	2	COM47	82	SB114	162	SC87	242	SA61	322	SB34	402	SC7	482	COM80	562
VCOMH	3	COM45	83	SA114	163	SB87	243	SC60	323	SA34	403	SB7	483	COM82	563
VDDIO	4	COM43	84	SC113	164	SA87	244	SB60	324	SC33	404	SA7	484	COM84	564
VSL	5	COM41	85	SB113	165	SC86	245	SA60	325	SB33	405	SC6	485	COM86	565
D17	6	COM39	86	SA113	166	SB86	246	SC59	326	SA33	406	SB6	486	COM88	566
D16	7	COM37	87	SC112	167	SA86	247	SB59	327	SC32	407	SA6	487	COM90	567
D15	8	COM35	88	SB112	168	SC85	248	SA59	328	SB32	408	SC5	488	COM92	568
D14	9	COM33	89	SA112	169	SB85	249	SC58	329	SA32	409	SB5	489	COM94	569
D13	10	COM31	90	SC111	170	SA85	250	SB58	330	SC31	410	SA5	490	COM96	570
D12	11	COM29	91	SB111	171	SC84	251	SA58	331	SB31	411	SC4	491	COM98	571
D11	12	COM27	92	SA111	172	SB84	252	SC57	332	SA31	412	SB4	492	COM100	572
D10	13	COM25	93	SC110	173	SA84	253	SB57	333	SC30	413	SA4	493	COM102	573
D9	14	COM23	94	SB110	174	SC83	254	SA57	334	SB30	414	SC3	494	COM104	574
D8	15	COM21	95	SA110	175	SB83	255	SC56	335	SA30	415	SB3	495	COM106	575
D7	16	COM19	96	SC109	176	SA83	256	SB56	336	SC29	416	SA3	496	COM108	576
D6	17	COM17	97	SB109	177	SC82	257	SA56	337	SB29	417	SC2	497	COM110	577
D5	18	COM15	98	SA109	178	SB82	258	SC55	338	SA29	418	SB2	498	COM112	578
D4	19	COM13	99	SC108	179	SA82	259	SB55	339	SC28	419	SA2	499	COM114	579
D3	20	COM11	100	SB108	180	SC81	260	SA55	340	SB28	420	SC1	500	COM116	580
D2	21	COM9	101	SA108	181	SB81	261	SC54	341	SA28	421	SB1	501	COM118	581
D1	22	COM7	102	SC107	182	SA81	262	SB54	342	SC27	422	SA1	502	COM120	582
D0	23	COM5	103	SB107	183	SC80	263	SA54	343	SB27	423	SC0	503	COM122	583
E	24	COM3	104	SA107	184	SB80	264	SC53	344	SA27	424	SB0	504	COM124	584
R/W#	25	COM1	105	SC106	185	SA80	265	SB53	345	SC26	425	SA0	505	COM126	585
BS0	26	NC	106	SB106	186	SC79	266	SA53	346	SB26	426	NC	506	NC	586
BS1	27	NC	107	SA106	187	SB79	267	SC52	347	SA26	427	NC	507	NC	587
BS2	28	NC	108	SC105	188	SA79	268	SB52	348	SC25	428	NC	508		
CS#	29	NC	109	SB105	189	SC78	269	SA52	349	SB25	429	NC	509		
D/C#	30	NC	110	SA105	190	SB78	270	SC51	350	SA25	430	NC	510		
RES#	31	NC	111	SC104	191	SA78	271	SB51	351	SC24	431	NC	511		
IREF	32	NC	112	SB104	192	SC77	272	SA51	352	SB24	432	NC	512		
VBREF	33	NC	113	SA104	193	SB77	273	SC50	353	SA24	433	NC	513		
RESE	34	NC	114	SC103	194	SA77	274	SB50	354	SC23	434	NC	514		
FB	35	NC	115	SB103	195	SC76	275	SA50	355	SB23	435	NC	515		
VDD	36	NC	116	SA103	196	SB76	276	SC49	356	SA23	436	NC	516		
GDR	37	NC	117	SC102	197	SA76	277	SB49	357	SC22	437	NC	517		
VSS	38	NC	118	SB102	198	SC75	278	SA49	358	SB22	438	NC	518		
NC	39	NC	119	SA102	199	SB75	279	SC48	359	SA22	439	NC	519		
NC	40	NC	120	SC101	200	SA75	280	SB48	360	SC21	440	NC	520		
NC	41	NC	121	SB101	201	SC74	281	SA48	361	SB21	441	NC	521		
COM127	42	SC127	122	SA101	202	SB74	282	SC47	362	SA21	442	COM0	522		
COM125	43	SB127	123	SC100	203	SA74	283	SB47	363	SC20	443	COM2	523		
COM123	44	SA127	124	SB100	204	SC73	284	SA47	364	SB20	444	COM4	524		
COM121	45	SC126	125	SA100	205	SB73	285	SC46	365	SA20	445	COM6	525		
COM119	46	SB126	126	SC99	206	SA73	286	SB46	366	SC19	446	COM8	526		
COM117	47	SA126	127	SB99	207	SC72	287	SA46	367	SB19	447	COM1	527		
COM115	48	SC125	128	SA99	208	SB72	288	SC45	368	SA19	448	COM1	528		
COM113	49	SB125	129	SC98	209	SA72	289	SB45	369	SC18	449	COM1	529		
COM111	50	SA125	130	SB98	210	SC71	290	SA45	370	SB18	450	COM1	530		
COM109	51	SC124	131	SA98	211	SB71	291	SC44	371	SA18	451	COM1	531		
COM107	52	SB124	132	SC97	212	SA71	292	SB44	372	SC17	452	COM2	532		
COM105	53	SA124	133	SB97	213	SC70	293	SA44	373	SB17	453	COM2	533		
COM103	54	SC123	134	SA97	214	SB70	294	SC43	374	SA17	454	COM2	534		
COM101	55	SB123	135	SC96	215	SA70	295	SB43	375	SC16	455	COM2	535		
COM99	56	SA123	136	SB96	216	SC69	296	SA43	376	SB16	456	COM2	536		
COM97	57	SC122	137	SA96	217	SB69	297	SC42	377	SA16	457	COM3	537		
COM95	58	SB122	138	SC95	218	SA69	298	SB42	378	SC15	458	COM3	538		
COM93	59	SA122	139	SB95	219	SC68	299	SA42	379	SB15	459	COM3	539		
COM91	60	SC121	140	SA95	220	SB68	300	SC41	380	SA15	460	COM3	540		
COM89	61	SB121	141	SC94	221	SA68	301	SB41	381	SC14	461	COM3	541		
COM87	62	SA121	142	SB94	222	SC67	302	SA41	382	SB14	462	COM4	542		
COM85	63	SC120	143	SA94	223	SB67	303	SC40	383	SA14	463	COM4	543		
COM83	64	SB120	144	SC93	224	SA67	304	SB40	384	SC13	464	COM4	544		
COM81	65	SA120	145	SB93	225	SC66	305	SA40	385	SB13	465	COM4	545		
COM79	66	SC119	146	SA93	226	SB66	306	SC39	386	SA13	466	COM4	546		
COM77	67	SB119	147	SC92	227	SA66	307	SB39	387	SC12	467	COM5	547		
COM75	68	SA119	148	SB92	228	SC65	308	SA39	388	SB12	468	COM5	548		
COM73	69	SC118	149	SA92	229	SB65	309	SC38	389	SA12	469	COM5	549		
COM71	70	SB118	150	SC91	230	SA65	310	SB38	390	SC11	470	COM5	550		
COM69	71	SA118	151	SB91	231	SC64	311	SA38	391	SB11	471	COM5	551		
COM67	72	SC117	152	SA91	232	SB64	312	SC37	392	SA11	472	COM6	552		
COM65	73	SB117	153	SC90	233	SA64	313	SB37	393	SC10	473	COM6	553		
COM63	74	SA117	154	SB90	234	SC63	314	SA37	394	SB10	474	COM6	554		
COM61	75	SC116	155	SA90	235	SB63	315	SC36	395	SA10	475	COM6	555		
COM59	76	SB116	156	SC89	236	SA63	316	SB36	396	SC9	476	COM6	556		
COM57	77	SA116	157	SB89	237	SC62	317	SA36	397	SB9	477	COM7	557		
COM55	78	SC115	158	SA89	238	SB62	318	SC35	398	SA9	478	COM7	558		
COM53	79	SB115	159	SC88	239	SA62	319	SB35	399	SC8	479	COM7	559		
COM51	80	SA115	160	SB88	240	SC61	320	SA35	400	SB8	480	COM7	560		

6.2 SSD1339U3 Pin Assignment

Figure 6-2 : SSD1339U3 pin assignment

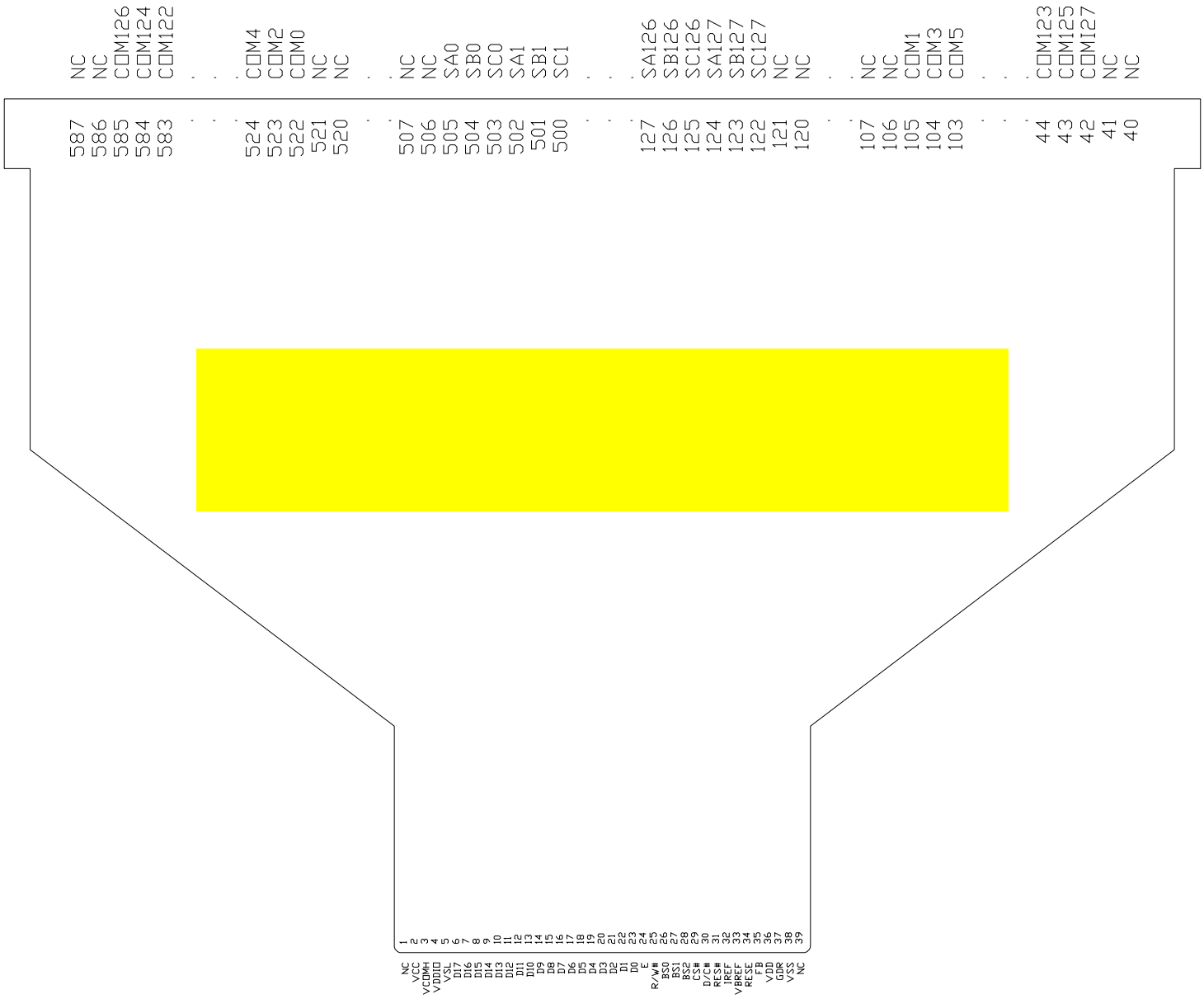


Table 6-2 - SSD1339U3 pin assignment

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
NC	1	COM49	81	SC114	161	SA88	241	SB61	321	SC34	401	SA8	481	COM78	561
VCC	2	COM47	82	SB114	162	SC87	242	SA61	322	SB34	402	SC7	482	COM80	562
VCOMH	3	COM45	83	SA114	163	SB87	243	SC60	323	SA34	403	SB7	483	COM82	563
VDDIO	4	COM43	84	SC113	164	SA87	244	SB60	324	SC33	404	SA7	484	COM84	564
VSL	5	COM41	85	SB113	165	SC86	245	SA60	325	SB33	405	SC6	485	COM86	565
D17	6	COM39	86	SA113	166	SB86	246	SC59	326	SA33	406	SB6	486	COM88	566
D16	7	COM37	87	SC112	167	SA86	247	SB59	327	SC32	407	SA6	487	COM90	567
D15	8	COM35	88	SB112	168	SC85	248	SA59	328	SB32	408	SC5	488	COM92	568
D14	9	COM33	89	SA112	169	SB85	249	SC58	329	SA32	409	SB5	489	COM94	569
D13	10	COM31	90	SC111	170	SA85	250	SB58	330	SC31	410	SA5	490	COM96	570
D12	11	COM29	91	SB111	171	SC84	251	SA58	331	SB31	411	SC4	491	COM98	571
D11	12	COM27	92	SA111	172	SB84	252	SC57	332	SA31	412	SB4	492	COM100	572
D10	13	COM25	93	SC110	173	SA84	253	SB57	333	SC30	413	SA4	493	COM102	573
D9	14	COM23	94	SB110	174	SC83	254	SA57	334	SB30	414	SC3	494	COM104	574
D8	15	COM21	95	SA110	175	SB83	255	SC56	335	SA30	415	SB3	495	COM106	575
D7	16	COM19	96	SC109	176	SA83	256	SB56	336	SC29	416	SA3	496	COM108	576
D6	17	COM17	97	SB109	177	SC82	257	SA56	337	SB29	417	SC2	497	COM110	577
D5	18	COM15	98	SA109	178	SB82	258	SC55	338	SA29	418	SB2	498	COM112	578
D4	19	COM13	99	SC108	179	SA82	259	SB55	339	SC28	419	SA2	499	COM114	579
D3	20	COM11	100	SB108	180	SC81	260	SA55	340	SB28	420	SC1	500	COM116	580
D2	21	COM9	101	SA108	181	SB81	261	SC54	341	SA28	421	SB1	501	COM118	581
D1	22	COM7	102	SC107	182	SA81	262	SB54	342	SC27	422	SA1	502	COM120	582
D0	23	COM5	103	SB107	183	SC80	263	SA54	343	SB27	423	SC0	503	COM122	583
E	24	COM3	104	SA107	184	SB80	264	SC53	344	SA27	424	SB0	504	COM124	584
R/W#	25	COM1	105	SC106	185	SA80	265	SB53	345	SC26	425	SA0	505	COM126	585
BS0	26	NC	106	SB106	186	SC79	266	SA53	346	SB26	426	NC	506	NC	586
BS1	27	NC	107	SA106	187	SB79	267	SC52	347	SA26	427	NC	507	NC	587
BS2	28	NC	108	SC105	188	SA79	268	SB52	348	SC25	428	NC	508		
CS#	29	NC	109	SB105	189	SC78	269	SA52	349	SB25	429	NC	509		
D/C#	30	NC	110	SA105	190	SB78	270	SC51	350	SA25	430	NC	510		
RES#	31	NC	111	SC104	191	SA78	271	SB51	351	SC24	431	NC	511		
IREF	32	NC	112	SB104	192	SC77	272	SA51	352	SB24	432	NC	512		
VBREF	33	NC	113	SA104	193	SB77	273	SC50	353	SA24	433	NC	513		
RESE	34	NC	114	SC103	194	SA77	274	SB50	354	SC23	434	NC	514		
FB	35	NC	115	SB103	195	SC76	275	SA50	355	SB23	435	NC	515		
VDD	36	NC	116	SA103	196	SB76	276	SC49	356	SA23	436	NC	516		
GDR	37	NC	117	SC102	197	SA76	277	SB49	357	SC22	437	NC	517		
VSS	38	NC	118	SB102	198	SC75	278	SA49	358	SB22	438	NC	518		
NC	39	NC	119	SA102	199	SB75	279	SC48	359	SA22	439	NC	519		
NC	40	NC	120	SC101	200	SA75	280	SB48	360	SC21	440	NC	520		
NC	41	NC	121	SB101	201	SC74	281	SA48	361	SB21	441	NC	521		
COM127	42	SC127	122	SA101	202	SB74	282	SC47	362	SA21	442	COM0	522		
COM125	43	SB127	123	SC100	203	SA74	283	SB47	363	SC20	443	COM2	523		
COM123	44	SA127	124	SB100	204	SC73	284	SA47	364	SB20	444	COM4	524		
COM121	45	SC126	125	SA100	205	SB73	285	SC46	365	SA20	445	COM6	525		
COM119	46	SB126	126	SC99	206	SA73	286	SB46	366	SC19	446	COM8	526		
COM117	47	SA126	127	SB99	207	SC72	287	SA46	367	SB19	447	COM1	527		
COM115	48	SC125	128	SA99	208	SB72	288	SC45	368	SA19	448	COM1	528		
COM113	49	SB125	129	SC98	209	SA72	289	SB45	369	SC18	449	COM1	529		
COM111	50	SA125	130	SB98	210	SC71	290	SA45	370	SB18	450	COM1	530		
COM109	51	SC124	131	SA98	211	SB71	291	SC44	371	SA18	451	COM1	531		
COM107	52	SB124	132	SC97	212	SA71	292	SB44	372	SC17	452	COM2	532		
COM105	53	SA124	133	SB97	213	SC70	293	SA44	373	SB17	453	COM2	533		
COM103	54	SC123	134	SA97	214	SB70	294	SC43	374	SA17	454	COM2	534		
COM101	55	SB123	135	SC96	215	SA70	295	SB43	375	SC16	455	COM2	535		
COM99	56	SA123	136	SB96	216	SC69	296	SA43	376	SB16	456	COM2	536		
COM97	57	SC122	137	SA96	217	SB69	297	SC42	377	SA16	457	COM3	537		
COM95	58	SB122	138	SC95	218	SA69	298	SB42	378	SC15	458	COM3	538		
COM93	59	SA122	139	SB95	219	SC68	299	SA42	379	SB15	459	COM3	539		
COM91	60	SC121	140	SA95	220	SB68	300	SC41	380	SA15	460	COM3	540		
COM89	61	SB121	141	SC94	221	SA68	301	SB41	381	SC14	461	COM3	541		
COM87	62	SA121	142	SB94	222	SC67	302	SA41	382	SB14	462	COM4	542		
COM85	63	SC120	143	SA94	223	SB67	303	SC40	383	SA14	463	COM4	543		
COM83	64	SB120	144	SC93	224	SA67	304	SB40	384	SC13	464	COM4	544		
COM81	65	SA120	145	SB93	225	SC66	305	SA40	385	SB13	465	COM4	545		
COM79	66	SC119	146	SA93	226	SB66	306	SC39	386	SA13	466	COM4	546		
COM77	67	SB119	147	SC92	227	SA66	307	SB39	387	SC12	467	COM5	547		
COM75	68	SA119	148	SB92	228	SC65	308	SA39	388	SB12	468	COM5	548		
COM73	69	SC118	149	SA92	229	SB65	309	SC38	389	SA12	469	COM5	549		
COM71	70	SB118	150	SC91	230	SA65	310	SB38	390	SC11	470	COM5	550		
COM69	71	SA118	151	SB91	231	SC64	311	SA38	391	SB11	471	COM5	551		
COM67	72	SC117	152	SA91	232	SB64	312	SC37	392	SA11	472	COM6	552		
COM65	73	SB117	153	SC90	233	SA64	313	SB37	393	SC10	473	COM6	553		
COM63	74	SA117	154	SB90	234	SC63	314	SA37	394	SB10	474	COM6	554		
COM61	75	SC116	155	SA90	235	SB63	315	SC36	395	SA10	475	COM6	555		
COM59	76	SB116	156	SC89	236	SA63	316	SB36	396	SC9	476	COM6	556		
COM57	77	SA116	157	SB89	237	SC62	317	SA36	397	SB9	477	COM7	557		
COM55	78	SC115	158	SA89	238	SB62	318	SC35	398	SA9	478	COM7	558		
COM53	79	SB115	159	SC88	239	SA62	319	SB35	399	SC8	479	COM7	559		
COM51	80	SA115	160	SB88	240	SC61	320	SA35	400	SB8	480	COM7	560		

7 PIN DESCRIPTION

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin

Table 7-1 : Pin Description

Pin Name	Pin Type	Description
RES#	I	This pin is reset signal input. When the pin is LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DDIO}) during normal operation.
CS#	I	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled LOW.
D/C#	I	This pin is Data/Command control pin. When the pin is pulled HIGH (i.e. connect to V_{DDIO}), the data at D[17:0] is treated as data. When the pin is pulled LOW, the data at D[17:0] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams in Figure 13-1, Figure 13-2 and Figure 13-3.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DDIO}) and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled LOW and the chip is selected.
R/W#(WR#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DDIO}) and write mode will be carried out when this pin is pulled LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
D[17-0]	IO	These pins are 18-bit bi-directional data bus to be connected to the microprocessor's data bus.
BS[3:0]	I	MCU bus interface selection pins. Please refer to Table 7-2 for the details of the selection.
V_{DDIO}	P	This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have VIH reference to V_{DDIO} . When I/O signal pins (BS0, BS1, BS2, BS3, MS, CLS, D0-D17, control signals…) pull HIGH, they should be connected to V_{DDIO} .
V_{DD}	P	Power Supply pin. It must be connected to external source.
V_{SS}	P	Ground. It also acts as a reference for the logic pins. It must be connected to external ground.
CL	IO	This pin is the system clock input. When internal clock is enabled (i.e. CLS is pulled HIGH), this pin should be left open. Nothing should be connected to this pin. When internal oscillator is disabled (i.e. CLS is pulled LOW), this pin receives display clock signal from external clock source.
MS	I	This pin must be connected to V_{DDIO} to enable the chip.

Pin Name	Pin Type	Description
CLS	I	This pin is internal clock enable. When this pin is pulled HIGH (i.e. connect to V_{DDIO}), internal oscillator is selected. The internal clock will be disabled when it is pulled LOW, an external clock source must be connected to CL pin for normal operation.
V_{DDB}	P	This is the power supply pin for the internal buffer of the DC-DC voltage converter. It must be connected to V_{DD} when the converter is used. It is also recommended to connect this pin to V_{DD} when the converter is not used to avoid floating node.
V_{SSB}	P	This is the GND pin for the internal buffer of the DC-DC voltage converter. It must be connected to V_{SS} when the converter is used. It is also recommended to connect this pin to V_{SS} when the converter is not used to avoid floating node.
GDR	O	This output pin drives the gate of the external NMOS of the booster circuit. This pin can be left open when the converter is not used.
RESE	I	This pin connects to the source current pin of the external NMOS of the booster circuit. This pin can be left open when the converter is not used.
FB	I	This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (V_{CC}). This pin can be left open when the converter is not used.
BGGND	P	This is a ground pin for analog circuits. It must be connected to external ground.
V_{BREF}	P	This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typ. 1uF, should be connected to V_{SS}. This pin can be left open when the converter is not used.
V_{CC}	P	This is the most positive voltage supply pin of the chip. It is supplied either by external HIGH voltage source or internal booster
V_{COMH}	O	A capacitor, with recommended value 4.7uF should be connected between this pin and V_{SS}. No external power supply is allowed to connect to this pin.
V_{REF}	P	This pin is the reference for OLED driving voltages like V_{PA}, V_{PB}, V_{PC} and V_{COMH}. It can be either supplied externally or connected to V_{CC} ($V_{REF} \leq V_{CC}$).
V_{PA}, V_{PB}, V_{PC}	P	These pins are the driving voltages for OLED driving segment pins SA0-SA131, SB0-SB131 and SC0-SC131 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, V_{PA}, V_{PB}, V_{PC} pins should be left open.
I_{REF}	I	This pin is the segment output current reference pin. I_{SEG} of each color is derived from I_{REF} I_{SEG} = (Contrast / 256) * I_{REF} * scale factor Contrast is set by command C1h Scale factor = master current control register setting (C7h) + 1, i.e., with value from 1~16. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA.
VSL	P	This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, refer to Figure 10-6 for the pin connection.

Pin Name	Pin Type	Description
VCL	P	This is common voltage reference pin. This pin should be connected to V_{SS} externally.
COM0-COM131	O	These pins provide the Common switch signals to the OLED panel. These pins are in HIGH impedance state when display is OFF.
SA0-SA131, SB0-SB131, SC0-SC131	O	These pins provide the OLED segment driving signals. These pins are in HIGH impedance state when display is OFF. The 396 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.
COMX	O	These two pins provide the Common switch signals for soft icon line to the OLED panel. These pins are in high impedance state when display is OFF.
TR0 ~TR8, VMONA, ICASA, ICASB, ICASC, GPIO0, GPIO1, M, DOF#	-	These are reserved pins. No connection is necessary and should be left open individually.
NC	-	No connection pins. They should be left open individually.

Table 7-2 : MCU Bus Interface Pin Selection

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	6800-parallel interface (16 bit)	8080-parallel interface (16 bit)	Serial interface
BS0	0	0	1	1	0
BS1	0	1	0	1	0
BS2	1	1	1	1	0
BS3	0	0	0	0	0

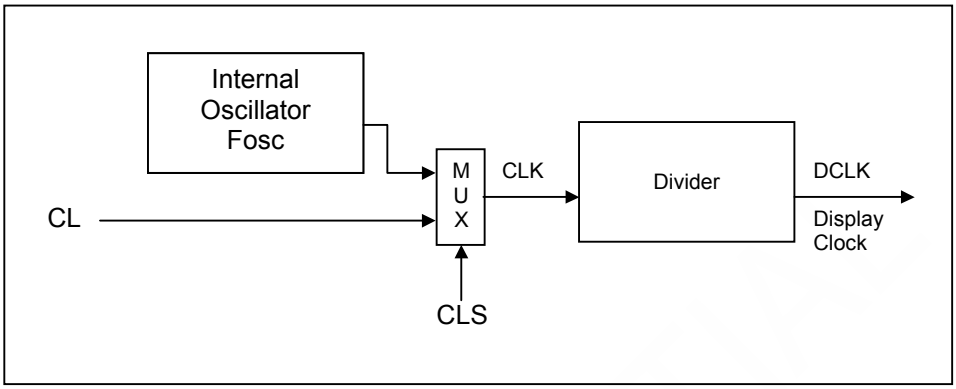
	6800-parallel interface (9 bit)	8080-parallel interface (9 bit)	6800-parallel interface (18 bit)	8080-parallel interface (18 bit)
BS0	0	0	1	1
BS1	0	1	0	1
BS2	1	1	1	1
BS3	1	1	1	1

Note
(1) Unlike BS0, BS1 and BS2 are controlled by hardware connection, BS3 is controlled by software command, A0.

8 FUNCTIONAL BLOCK DISCRIPTIONS

8.1 Oscillator Circuit and Display Time Generator

Figure 8-1 : Oscillator Circuit



This module is an On-Chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled high, internal oscillator is chosen. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command B3h.

In some COF packages of SSD1339, CLS pin is tied to high internally and the internal oscillator is selected in these packages.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor can be programmed from 1 to 16 by command B3h.

8.2 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 132x132 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h

8.3 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

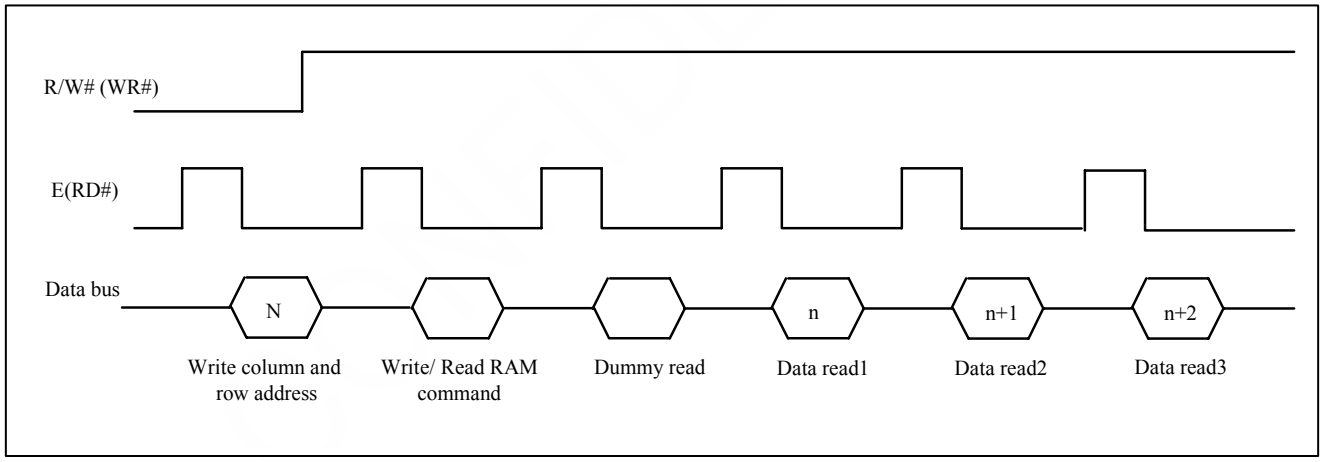
If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[17:0]is interpreted as a Command and it will be decoded and be written to the corresponding command register.

8.4 MPU Parallel 6800-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]) or 8 bi-directional data pins (D[7:0]), R/W#(WR#), D/C#, E (RD#) and CS#. R/W#(WR#) input HIGH indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. RW(WR#) input LOW indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E(RD#) input serves as data latch signal (clock) when HIGH provided that CS# is LOW and HIGH respectively. Refer to Figure 13-1 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-2 below.

Figure 8-2 : Display data read back procedure - insertion of dummy read



8.5 MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]) or 8 bi-directional data pins (D[7:0]), E (RD#), R/W#(WR#), D/C# and CS#. The E(RD#) input serves as data read latch signal (clock) when LOW, provided that CS# is LOW and HIGH respectively. Display data or status register read is controlled by D/C#.

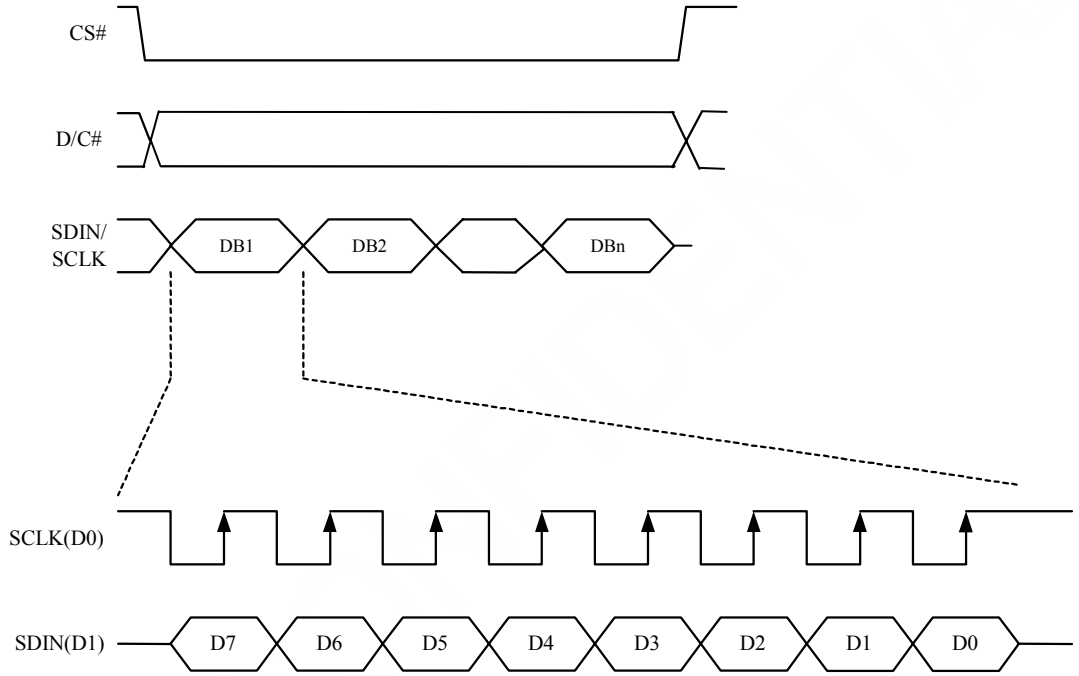
R/W#(WR#) input serves as data write latch signal (clock) when HIGH provided that CS# is LOW and HIGH respectively. Display data or command register write is controlled by D/C#. Refer to Figure 13-2 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

8.6 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In this mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. D3 to D17, E and R/W# pins can be connected to external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Figure 8-3 : Write procedure in SPI mode

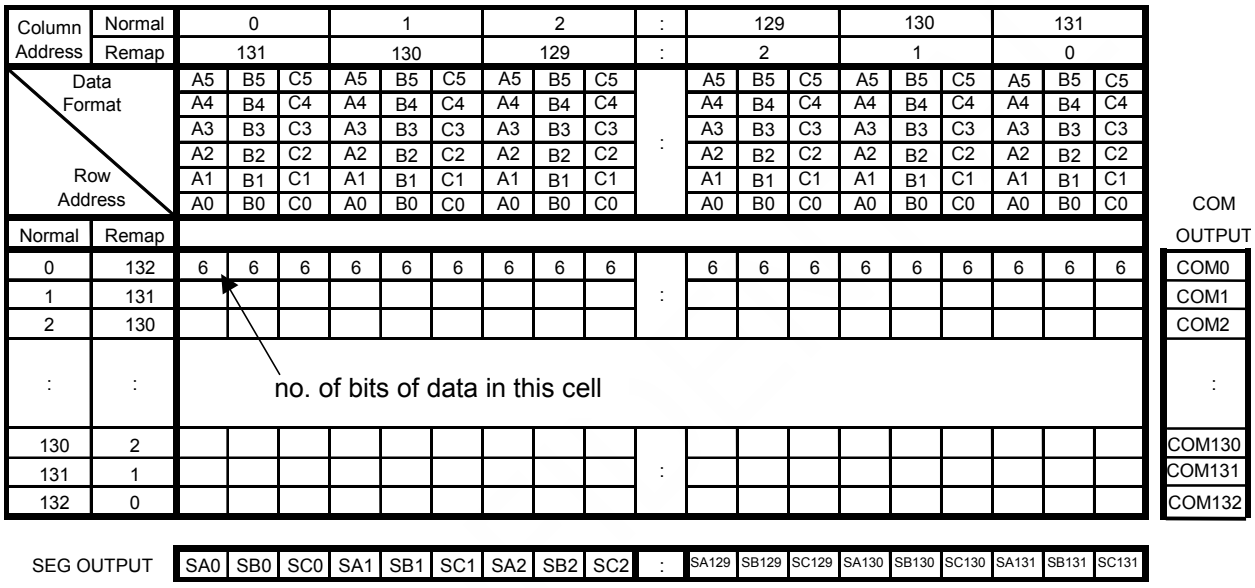


8.7 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 133 x 18bits.
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

Figure 8-4 : Graphic Display Data RAM Structure



8.7.1 Data access in 262k colors mode

In 262k colors depth mode, there are different MCU interface communication modes to access graphic display data RAM in OLED driver.

For 18 bits mode, the communication is made up of one session of 18 data bits. MCU transmits all bits to write ***one*** 18-bit pixel data into OLED driver. This 18-bit mode can be selected by setting the A[3] bit in command A0 to 1.

Figure 8-5 : 262k color depth data writing sequence in 18-bit MCU interface

Bit	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data bits	C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

For the 1st option of the two 16-bit modes, the communication is divided into two sessions of 16 data bits. MCU transmits two 16-bit words to write ***one*** 18-bit pixel data into OLED driver. Mode 1 is selected by setting A0h register A[7:6] bits to 10b. In below, A1, B1, C1 are pixel bits for color A, B and C, and "X" stands for don't care value.

Figure 8-6 : 262k color depth data writing sequence in 16-bit MCU interface in Option 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	X	X	X	X	X	X	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$
2nd word	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$

For the 2nd option of the 16-bit modes, the communication is divided into three sessions of 16 data bits. MCU transmits three 16-bit words to write ***two*** 18-bit pixels data into OLED driver. Option 2 is selected by setting A0h register A[7:6] bits to 11b. In below, A1, B1, C1 are first data pixel bits, and A2, B2, C2 are second data pixel bits.

Figure 8-7 : 262k color depth data writing sequence in 16-bit MCU interface in Option 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
2nd word	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$
3th word	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$

For 9-bit modes, the communication is divided into two sessions of 9 data bits. MCU transmits two 9 data bits to write ***one*** 18-bit pixel data into OLED driver. This 9-bit mode can be selected by setting the A[3] bit in command A0 to 1.

Figure 8-8 : 262k color depth graphic display data writing sequence in 9-bit MCU interface

Bit	8	7	6	5	4	3	2	1	0
1st 9 Data bits	C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
2nd 9 Data bits	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

In 8-bit MCU interface, the communication session is divided into three times. MCU transmit three 8-bit bytes to write one 18-bit pixel data into OLED driver.

Figure 8-9 : 262k color depth graphic display data writing sequence in 8-bit MCU interface

Bit	7	6	5	4	3	2	1	0
1st byte	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$
2nd byte	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
3rd byte	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$

8.7.2 Data access in 65k colors mode

Writing a 65K pixel in 16-bit MCU interface involves one session as follows.

Figure 8-10 : 65k color depth graphic display data writing sequence in 16-bit MCU interface

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$

The sequence of sending 65K color depth pixel in 8-bit MCU interface is divided into two 8-bit sessions as shown below.

Figure 8-11 : 65k color depth graphic display data writing sequence in 8-bit MCU interface

Bit	7	6	5	4	3	2	1	0
1st byte	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	$B1_5$	$B1_4$	$B1_3$
2nd byte	$B1_2$	$B1_1$	$B1_0$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$

With reference to Figure 8-4 conventions, in writing the data into graphic display data RAM, the bit positions filled by the input data for each color is shown below.

Figure 8-12 : Display data RAM writing position for color A, B and C data input in 65k color mode

Color A

Bit Position	A5	A4	A3	A2	A1	A0
Input Data	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	$A1_4$

Color B

Bit Position	B5	B4	B3	B2	B1	B0
Input Data	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$

Color C

Bit Position	C5	C4	C3	C2	C1	C0
Input Data	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	$C1_4$

In data RAM, each data occupies 6-bit. However, color A and C have 5-bit length only in 65k color mode. Therefore, RAM positions A0 and C0 are empty originally. These emptied positions are filled as shown above to increase color A and C to 6-bit length in display data RAM.

8.7.3 Data access in 256 colors mode

In 256-color mode, each pixel is composed of 8-bit. Only 8-bit MCU interface is available to access display data RAM. The communication session is done in 1 time by writing 8-bit data into RAM.

Figure 8-13 : 256 Color Depth Graphic Display Data Writing Sequence in 8-bit MCU Interface

Bit	7	6	5	4	3	2	1	0
1st byte	$C1_2$	$C1_1$	$C1_0$	$B1_2$	$B1_1$	$B1_0$	$A1_1$	$A1_0$

With reference to Figure 8-4 conventions, in writing the data into graphic display data RAM, the bit positions filled by the input data for each color is shown below.

Figure 8-14 : Display data RAM writing position for color A, B and C data input in 256 color mode

Color A

Bit Position	A5	A4	A3	A2	A1	A0
Input Data	$A1_1$	$A1_0$	$A1_1$	$A1_1$	$A1_1$	$A1_1$

Color B

Bit Position	B5	B4	B3	B2	B1	B0
Input Data	$B1_2$	$B1_1$	$B1_0$	$B1_2$	$B1_2$	$B1_2$

Color C

Bit Position	C5	C4	C3	C2	C1	C0
Input Data	$C1_2$	$C1_1$	$C1_0$	$C1_2$	$C1_2$	$C1_2$

In data RAM, each data occupies 6-bit. However, color B and C have 3-bit length and color A has 2-bit only in 256 color mode. Therefore, RAM positions B2~B0, C2~C0 and A3~A0 are empty originally. These emptied positions are filled as shown above to increase color A, B and C to 6-bit length in display data RAM.

8.8 Gray Scale and Gray Scale Table

Controlling the current pulse widths from the segment driver in the current drive phase produces the gray scale display. The gray scale table stores the corresponding pulse widths (PW0 ~ PW63) of the 64 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. Therefore, the brightness of each pixel is defined in the graphic display data RAM in term of pulse width in gray scale table.

This single gray scale table supports all the three colors A, B and C. The pulse widths are entered by software commands.

In graphic display data RAM, each color occupies 6-bit length. So color A, B and C each has 64 gray scale levels.

Figure 8-15 : Relation between graphic data RAM value and gray scale table entry for three colors

Color A, B, C RAM data (6 bits)	Gray Scale
0	GS 0
1	GS 1
2	GS 2
3	GS 3
4	GS 4
:	:
:	:
:	:
60	GS 60
61	GS 61
62	GS 62
63	GS 63

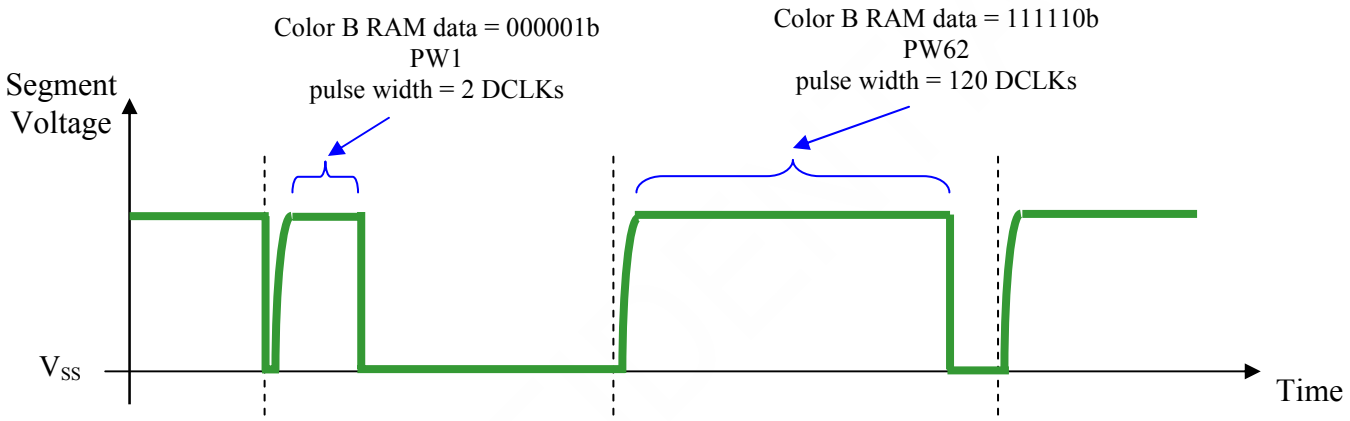
In 65k and 256 color modes, the length color data are less than 6 bits. They are expanded to 6-bit length as shown in Figure 8-12 and Figure 8-14 respectively.

The meaning of values inside data RAM with respect to the gray scale level is best to be illustrated in an example below.

Figure 8-16 : Illustration of relation between graphic display RAM value and gray scale control

Gray Scale (Pulse Width)	Value/DCLKs
PW0	0
PW1	2
PW2	5
:	:
PW62	120
PW63	125

Gray Scale Table



8.9 Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

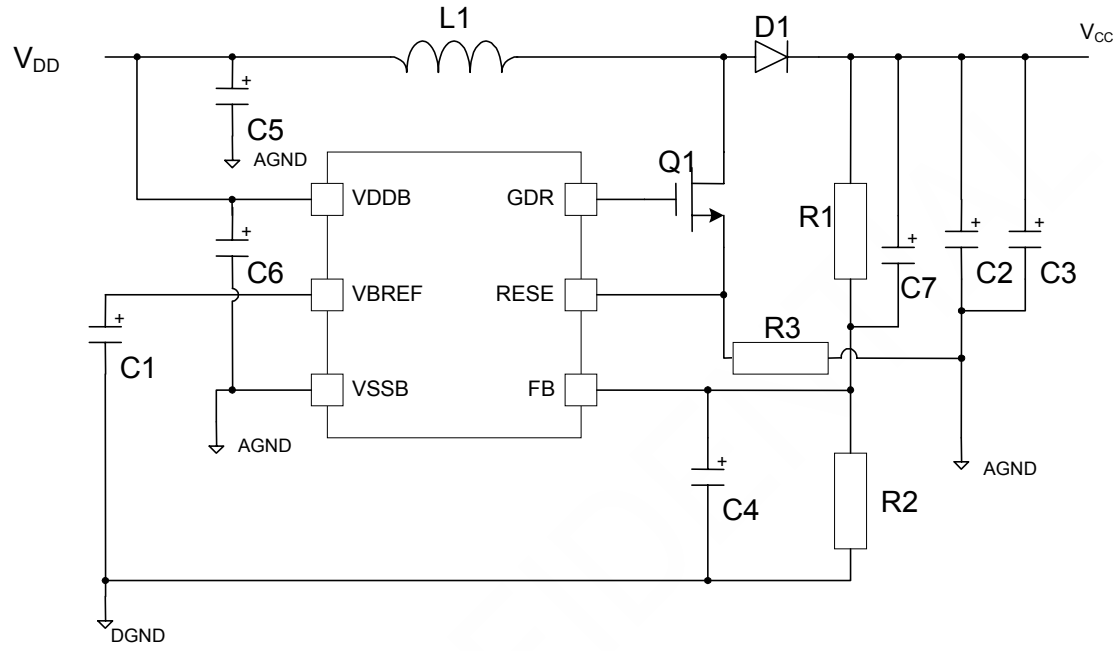
8.10 Segment Drivers/Common Drivers

Segment drivers deliver 396 current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps. Common drivers generate voltage scanning pulse.

8.11 DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for handheld applications. In SSD1339, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply V_{CC} from a LOW voltage supply input V_{DD}. V_{CC} is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V V_{DD} to generate V_{CC} of 12V @20mA ~ 30mA application.

Figure 8-17 :DC-DC voltage converter



Note

(1) All paths to AGND should be connected as short as possible

Passive components selection:

Components	Typical Value	Remark
L1	Inductor, 22uH	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
Q1	MOSFET	N-FET with LOW R_{DS}(on) and LOW Vth voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor	1%,1/10W
R3	Resistor, 1.5Ω	1%, 1/2W
C1	Capacitor, 1uF	16V
C2	Capacitor, 22uF	LOW ESR, 25V
C3	Capacitor, 1uF	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 uF	16V
C6	Capacitor, 0.1 ~ 1uF	16V
C7	Capacitor, 15nF	16V

The V_{CC} output voltage level can be adjusted by changing the R1 and R2 resistor values, the reference formula is:

$V_{CC} = 1.2 \times (R1+R2) / R2$

9 COMMAND TABLE

Table 9-1 : Command table

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 1 1	15 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=131] Range from 0 to 131
0 1 1	75 A[7:0] B[7:0]	0 A_7 B_7	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=131] Range from 0 to 131
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map / Color Depth(Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 131 is mapped to SEG0 A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A A[3]=0b, Disable 9/18-bit bus interface [reset] A[3]=1b, Enable 9/18-bit bus interface A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even A[7:6] Set Color Depth, 00b 256 color 01b 65K color, [reset] 10b 262k color, 8/9/18-bit,16 bit (1st option) MCU interface 11b 262k color, 16 - bit MCU interface (2nd option)
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~131. [reset=00h]

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-131. [reset=00h]
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4: All OFF A5: All ON (All pixels have GS15) A6 : Reset to normal display [reset] A7: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0 1	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 A_2	0 1	1 A_0	Master Configuration	A[0] = 0b Select external V_{CC} supply at master ON A[0] = 1b Select internal booster at master ON [reset] A[2] = 0b Select external pre-charge voltage source A[2] = 1b Select internal pre-charge voltage source [reset]
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AE = Sleep mode On (Display OFF) AF = Sleep mode OFF (Display ON)
0 1	B0 A[4:0]	1 0	0 0	1 0	1 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Power Saving Mode	A[4:0]: 00000b = Internal VSL Normal Power [reset] 10010b = Power Saving with Internal VSL 00101b = External VSL 10101b = Power Saving with External VSL **Note** (1) It is recommended to set A[4:0]=10101b (Power Saving with External VSL) for better performance, especially when high V_{CC} is used or high I_{cc} is consumed. (2) When external VSL is enabled, in order to avoid distortion in display pattern, an external circuit is needed to connect between VSL and V_{SS} as shown in Figure 10-6.
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) /Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 1~16 DCLK(s) clocks [reset=4h] A[7:4] Phase 2 period of 1~16 DCLK(s) clocks [reset=7h]
0 1	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0], divide by DIVSET+1 (i.e. 1 to 16) A[7:4] Oscillator frequency, frequency increase as level increase [reset=1001b]

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Look Up Table for Gray Scale Pulse width	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 …GS63 as below in unit of DCLK. A[7:0] : PW1, reset =1 DCLK B[7:0] : PW3, reset = 5 DCLK C[7:0] : PW5, reset = 9 DCLK : : AE[7:0] : PW61, reset = 121 DCLK AF[7:0] : PW63, reset = 123 DCLK where PW1 must > 0 PW3 must > PW1+1 PW5 must > PW3+1 **Note** (1) GS0 has no pre-charge and current drive stages. For GS2 GS4…GS62, they are derived by driver itself with: PWn = (PW_{n-1}+PW_{n+1})/2 Max pulse width is 125
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.AE[7:0]	AE_7	AE_6	AE_5	AE_4	AE_3	AE_2	AE_1	AE_0		
1	AF[7:0]	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0		
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: PW1 = 1 PW2 = 3 PW3 = 5 PW4 = 7 ... PW62 = 123 PW63 = 125
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage of Color A B C	A[7:0] Pre-charge Color A [reset = 00011100b] B[7:0] Pre-charge Color B [reset = 00011100b] C[7:0] Pre-charge Color C [reset = 00011100b] 00000000b 0.51*V_{REF} ..... 00011111b 0.84*V_{REF} 1xxxxxxxb connects to V_{COMH}
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	A[6:0] 0000000b 0.51*V_{REF} ..... 0011111b 0.84*V_{REF} [reset]
1	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 1 1 1	C1 A[7:0] B[7:0] C[7:0]	1 A_7 B_7 C_7	1 A_6 B_6 C_6	0 A_5 B_5 C_5	0 A_4 B_4 C_4	0 A_3 B_3 C_3	0 A_2 B_2 C_2	0 A_1 B_1 C_1	1 A_0 B_0 C_0	Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=10000000b] B[7:0] Contrast Value Color B [reset=10000000b] C[7:0] Contrast Value Color C [reset=10000000b]
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Contrast Current Control	A[3:0] : 0000 reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset = 1111b]
0 1	CA A[7:0]	1 A_7	1 A_6	0 A_5	0 A_4	1 A_3	0 A_2	1 A_1	0 A_0	Set MUX Ratio	A[7:0] mux ratio 16MUX ~ 132MUX, [reset=131], (Range from 15 to 131)
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Table 9-2 : Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	83	1	0	0	0	0	0	1	1	Draw Line	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Line Color - CCCCCBBB F[7:0] : Line Color - BBBAAAAA * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	84	1	0	0	0	0	1	0	0	Draw Rectangle	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Line Color - CCCCCBBB F[7:0] : Line Color - BBBAAAAA G[7:0] : Fill Color - CCCCCBBB H[7:0] : Fill Color - BBBAAAAA * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	G[7:0]	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	H[7:0]	H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	86	1	0	0	0	0	1	1	0	Draw Circle	A[7:0] : Column Address of Centre B[7:0] : Row Address of Centre C[7:0] : Radius D[7:0] : Line Color - CCCCCBBB E[7:0] : Line Color - BBBAAAAA F[7:0] : Fill Color - CCCCCBBB G[7:0] : Fill Color – BBBAAAAA
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	G[7:0]	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	8A	1	0	0	0	1	0	1	0	Copy	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Column Address of New Start F[7:0] : Row Address of New Start * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	8C	1	0	0	0	1	1	0	0	Dim Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	8E	1	0	0	0	1	1	1	0	Clear Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	92	1	0	0	1	0	0	1	0	Fill Enable / Disable	A0 0b : Disable Fill for Draw Rectangle/Circle Command [reset] 1b : Enable Fill for Draw Rectangle/Circle Command A4 0b : Disable reverse copy, reset] 1b : Enable reverse during copying. A5 0b : Disable x-wrap, [reset] 1b : Enable wrap around in x-direction during copying
1	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	96	1	0	0	1	0	1	1	0	Horizontal Scroll	A[7:0] : 1~124 horizontal offset in number of Column Invalid entry for value larger than 124 0 no horizontal scroll B[7:0] : start row address C[7:0] : number of rows to be H-scrolled B+C <= 132 D[7:0] : Reserved (reset=00h) E[1:0] : scrolling time interval 00b test mode 01b normal 10b slow 11b slowest Note : operates during display ON.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[1:0]	*	*	*	*	*	*	E_1	E_0		
0	9E	1	0	0	1	1	1	1	0	Stop Moving	Stop horizontal scroll
0	9F	1	0	0	1	1	1	1	1	Start Moving	Start horizontal scroll

Table 9-3 : Read Command Table

(D/C#=0, R/W# (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : "1" for Command lock D[6] : "1" for display OFF / "0" for display ON D[5] : Reserve D[4] : Reserve D[3] : Reserve D[2] : Reserve D[1] : Reserve D[0] : Reserve

Note
(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

9.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W# (WR#) pin and D/C# pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read.
Also, a dummy read is required before the first data read. To write data to the GDDRAM, input LOW to R/W# (WR#) pin and HIGH to D/C# pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Table 9-4 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Fundamental Commands

10.1.1 Set Column Address (15h)

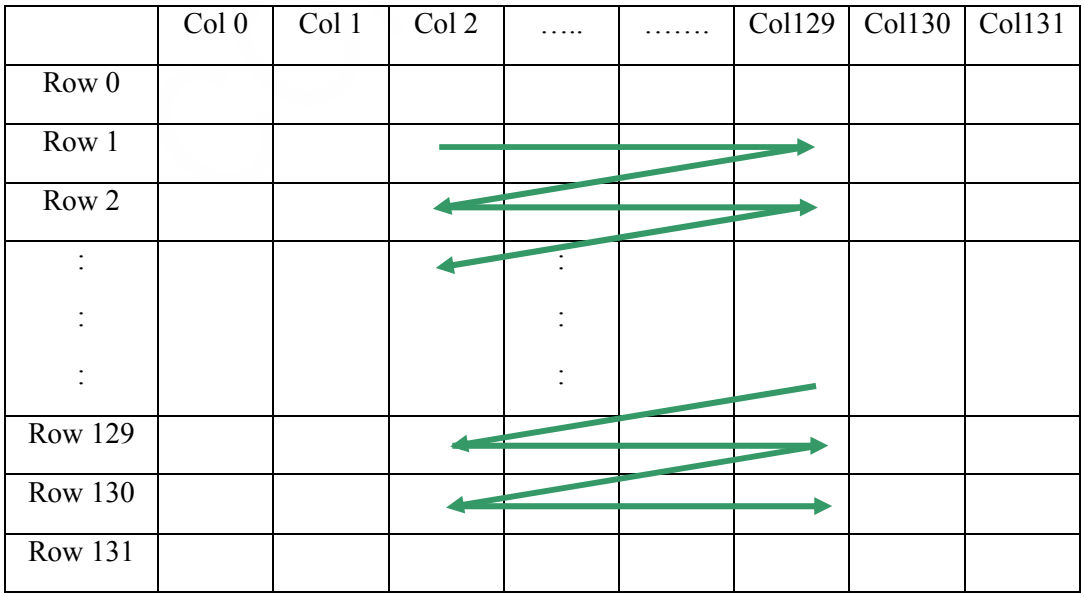
This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

10.1.2 Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 129, row start address is set to 1 and row end address is set to 130. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 129 and from row 1 to row 130 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation. Whenever the column address pointer finishes accessing the end column 129, it is reset back to column 2 and row address is automatically increased by 1. While the end row 130 and end column 129 RAM location is accessed, the row address is reset back to 1. The diagram below shows the way of column and row address pointer movement for this example.

Figure 10-1 : Example of column and row address pointer movement



10.1.3 Write RAM Command (5Ch)

After this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

10.1.4 Read RAM Command (5Dh)

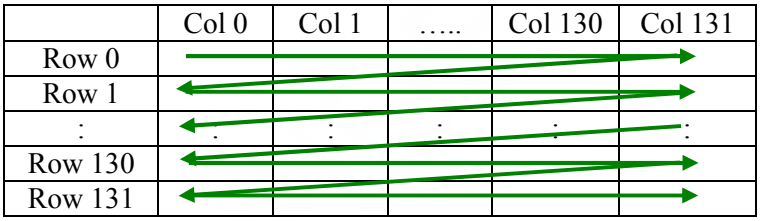
After this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

10.1.5 Set Re-map & Color Depth (A0h)

This command has multiple configurations and each bit setting is described as follows.

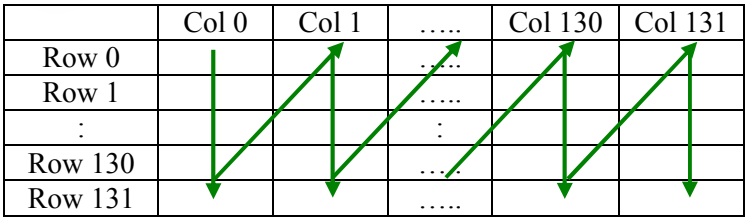
- Address increment mode (A[0])
  When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-2.

Figure 10-2 : Address pointer movement of horizontal address increment mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-3.

Figure 10-3 : Address pointer movement of vertical address increment mode



- Column Address Mapping (A[1])
  This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa.

- Color Remap (A[2])

This command bit is made for flexible layout of color sequence A → B → C or C → B → A.

- MCU interface selection (A[3])
  This command bit is made for setting the 6800 or 8080 parallel bus interface for to either 8/16-bit or 9/18-bit.

- COM Remap (A[4])
  This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.

- Odd even split of COM pins (A[5])
  This bit can set the odd even arrangement of COM pins.
  A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as
  COM131 COM129 .... COM 33 COM32..SC131..SA0..COM0 COM1.... COM30 COM31
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM131 COM129.... COM3 COM1..SC131..SA0..COM0 COM2.... COM60 COM62

- Display color mode (A[7:6])
  Select either 262k, 65k or 256 color mode.

  In 262k colors mode, if 16-bit MCU interface is selected, there are two communication modes. In mode 1, one pixel data in transmitted in two 16-bit words. In mode 2, one communication session is consisted of three 16-bit words to transmit two pixel data. Please refer to section 8.7.1 "Data access in 262k colors mode" for details. In all other 8/9/18-bit parallel or SPI MCU interfaces, there is no difference between mode 1 and mode 2 selections.

  The display RAM data format in different mode is described in section 8.7 "Graphic Display Data RAM (GDDRAM)".

10.1.6 Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 131. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 10-4 : Example of set display start line with no remap

	132	132	130	130	Mux ratio
COM Pin	0	4	0	4	Display start line
COM0	Row0	Row4	Row0	Row4	
COM1	Row1	Row5	Row1	Row5	
COM2	Row2	Row6	Row2	Row6	
COM3	Row3	Row7	Row3	Row7	
:	:	:	:	:	
:	:	:	:	:	
COM125	Row125	Row129	Row125	Row129	
COM126	Row126	Row130	Row126	Row130	
COM127	Row127	Row131	Row127	Row131	
COM128	Row128	Row0	Row128	Row0	
COM129	Row129	Row1	Row129	Row1	
COM130	Row130	Row2	-	-	
COM131	Row131	Row3	-	-	

10.1.7 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-131. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 10-5 : Example of set display offset with no remap

	132	132	130	130	Mux ratio
COM Pin	0	4	0	4	Display offset
COM0	Row0	Row4	Row0	Row4	
COM1	Row1	Row5	Row1	Row5	
COM2	Row2	Row6	Row2	Row6	
COM3	Row3	Row7	Row3	Row7	
:	:	:	:	:	
:	:	:	:	:	
COM125	Row125	Row129	Row125	Row129	
COM126	Row126	Row130	Row126	-	
COM127	Row127	Row131	Row127	-	
COM128	Row128	Row0	Row128	Row0	
COM129	Row129	Row1	Row129	Row1	
COM130	Row130	Row2	-	Row2	
COM131	Row131	Row3	-	Row3	

10.1.8 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

- Set Entire Display ON (A5h)
  Forces the entire display to be at "GS63" regardless of the contents of the display data RAM.
- Set Entire Display OFF (A4h)
  Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM.
- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….
- Normal Display (A6h)
  Reset the above effect and turn the data to ON at the corresponding gray level.

10.1.9 Master Configuration (ADh)

This command contains multiple bits to control several functionalities of the driver.

- Select DC-DC converter (A[0])
  0 = Disable selection of DC-DC converter and V_{CC} is supplied externally.
  1 [reset] = Enable selection of DC-DC converter to supply high voltage to V_{CC}. The output voltage of the converter is set by values of external resistors. Please refer to section "DC-DC Voltage Converter" for details.
- Select V_{COMH} supply (A[1])
  0 = Select external V_{COMH} voltage from V_{COMH} pin for the common waveform high voltage level supply. It is recommended to set the voltage of V_{COMH} such that the OLED pixel diode is not turned ON (prefer in reverse bias state) when the segment pin is either driven to V_{PA}, V_{PB} or V_{PC} level.

1 = Select internal V_{COMH} voltage generated by regulator from V_{REF}. The level of V_{COMH} can be programmed by command BEh.

- Select pre-charge voltage supply (A[2])
  0 = Select pre-charge voltage sources from external pins V_{PA}, V_{PB}, V_{PC} for color A, B and C respectively.
  1 = Select pre-charge voltage supply internally. The level of V_{PA}, V_{PB}, V_{PC} can be set by command BBh for color A, B and C respectively.

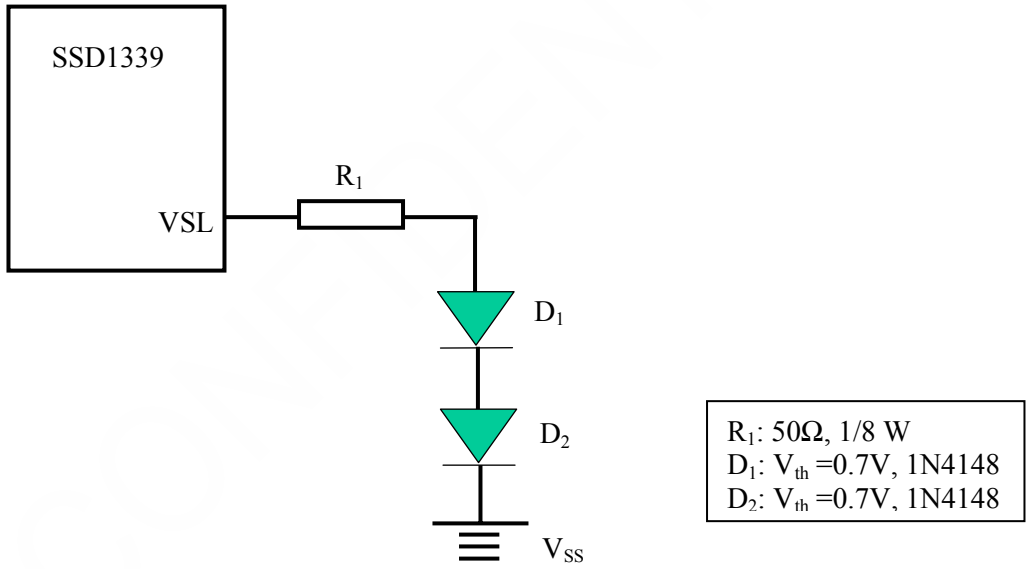
10.1.10 Set Sleep mode ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF. When the display is ON, the selected circuits by Set Master Configuration command will be turned ON. When the display is OFF, those circuits will be turned OFF and the segment and common output are in high impedance state.

10.1.11 Power Saving Mode (B0h)

This command is used in selecting normal powering mode or power saving mode, as well as to enable or disable external VSL. The following connection is recommended when external VSL is enabled.

Figure 10-6 : Recommended external VSL pin connection



It should be noticed that the VSL pin must not be left open when B0h command is set to "External VSL (0000 0101b)" or "Power Saving with External VSL (00010101b)", otherwise distortion in display pattern may occur.

10.1.12 Set Reset (Phase 1)/ Pre-charge (Phase 2) period (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 1 to 16 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 16 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_{PA}, V_{PB}, V_{PC} for color A, B and C respectively.

10.1.13 Front Clock Divider (DivSet)/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section "Oscillator Circuit and Display Time Generator" for the details of DCLK and CLK.
- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency setting available as shown below. The default value is 1101b.

10.1.14 Look Up Table for Gray Scale Pulse width (B8h)

This command is used to set the gray scale table for the display. Except gray scale entry 0, which is zero as it has no pre-charge and current drive, each odd entry gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter is the OLED pixel when it's turned ON. Please refer to section "Graphic Display Data RAM (GDDRAM)" for more detailed explanation of relation of display data RAM, gray scale table and the pixel brightness.

Following the command B8h, the user has to set the pulse width from PW1, PW3, PW5, …, PW59, PW61, PW63 one by one in sequence and complies the following conditions.

$$PW1 > 0; PW3 > PW1 + 1; PW5 > PW3 + 1; \ldots\ldots$$

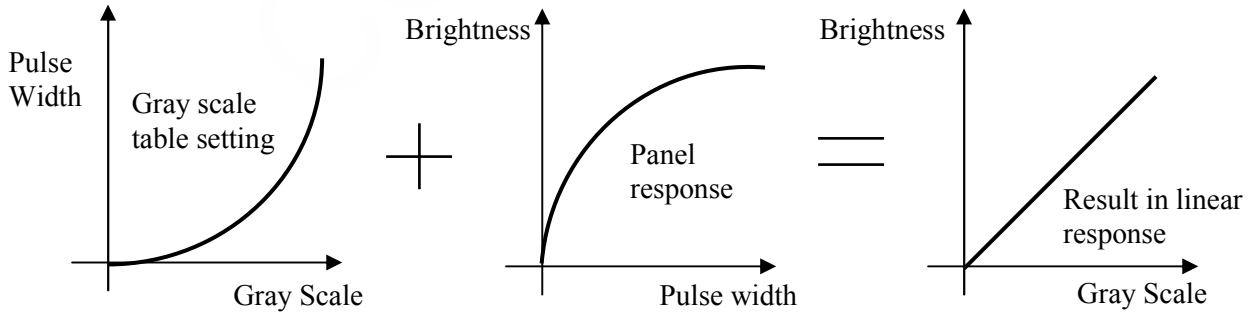
Afterwards, the driver automatically derives the pulse width of even entry of gray scale table PW2, PW4, …, PW62 with the formula like below.

$$PWn = (PWn\text{-}1 + PWn\text{+}1) / 2$$

For example, if PW1 = 3 DCLKs and PW3 = 7 DCLKs, PW2 = (3+7)/2 = 5 DCLKs

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Figure 10-7 : Example of gamma correction by gray scale table setting



10.1.15 Use Built-in Linear LUT (B9h)

This command reloads the preset linear gray scale table as PW1 = 1, PW2 = 3, PW3 = 5, …., PW62 = 123, PW63 = 125 DCLKs.

10.1.16 Set Pre-charge voltage of Color A, B and C (BBh)

This command is used to set V_{PA}, V_{PB} and V_{PC} phase 2 voltage level for color A, B and C respectively. The command is valid in condition that these voltages are selected to generate internally by command ADh. It can be programmed to set the pre-charge voltage reference to V_{REF} or V_{COMH}. Voltage level increases linearly when set value increases.

10.1.17 Set V_{COMH} (BEh)

This command sets the high voltage level of common pins, V_{COMH}, when it is selected to generate internally by command ADh. The level of V_{COMH} is programmed with reference to V_{REF}. Voltage level increases linearly when set value increases.

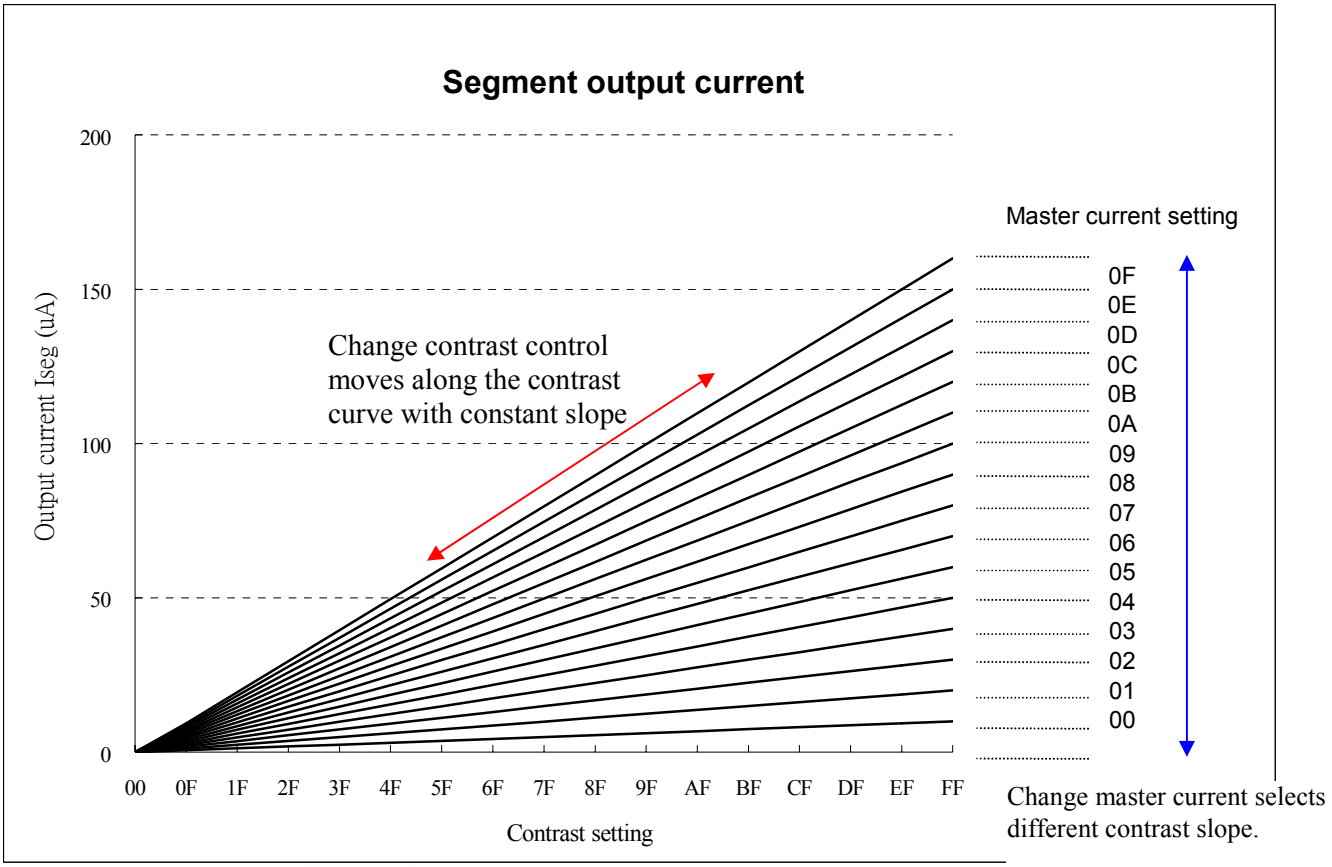
10.1.18 Contrast Current for Color A, B, C (C1h)

This command is to set Contrast Current of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 10-8. In many situations, the output brightness of color A, B and C pixels are different under the same segment current condition. The contrasts of color A, B and C are set such that the brightness of each color are the same on the OLED panel

10.1.19 Master Contrast Current Control (C7h)

This command is to control the segment output current by a scale factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000] to 16 [1111]. Reset is 16 [1111]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 10-8.

Figure 10-8 : Segment output current for different contrast control and master current setting



10.1.20 Set Multiplex Ratio (CAh)

This command switches default 1:132 multiplex mode to any multiplex mode from 16 to 132. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h.

10.1.21 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

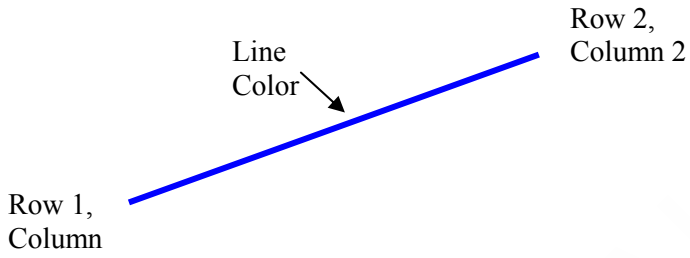
Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the "Lock" state. And the driver IC will then respond to the command and memory access.

10.2 Graphic Acceleration command set description

10.2.1 Draw Line (83h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

Figure 10-9 : Example of draw line command



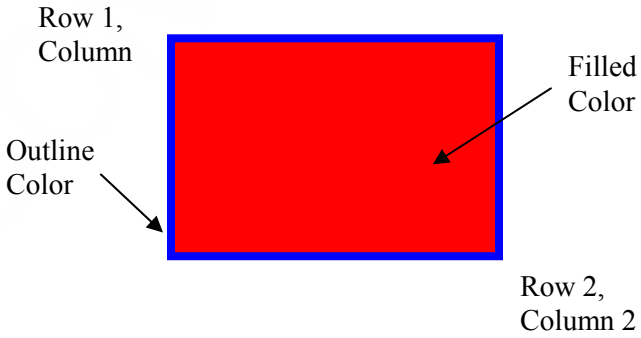
For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 83h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = 35d, 0d, 0d for blue color

10.2.2 Draw Rectangle (84h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.

Figure 10-10 : Example of draw rectangle command



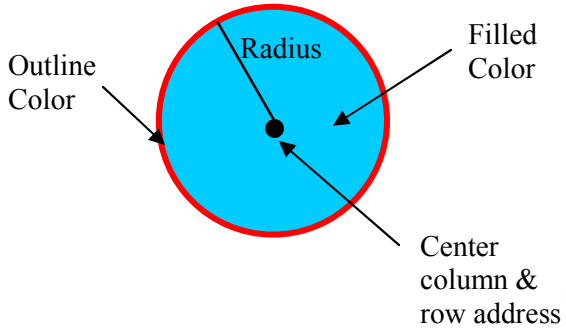
The following example illustrates the rectangle drawing command sequence.

1. Enter the “draw rectangle mode” by execute the command 84h
2. Set the starting column coordinates, Column 1. for example = 03h.
3. Set the starting row coordinates, Row 1. for example = 02h.
4. Set the finishing column coordinates, Column 2. for example = 12h
5. Set the finishing row coordinates, Row 2. for example = 15h
6. Set the outline color C, B and A. e.g., (28d, 0d, 0d) for blue color
7. Set the filled color C, B and A. e.g., (0d, 0d, 40d) for red color

10.2.3 Draw Circle (86h)

By providing the center coordination (column and row address) and radius length, specify the outline and fill area colors, a circle will be drawn with the colors specified.

Figure 10-11 : Example of draw circle command



The following example illustrates the circle drawing command sequence.

1. Enter the “draw circle mode” by execute the command 86h
2. Set the circle center column coordinates, for example = 03h.
3. Set the circle center row coordinates. for example = 10h.
4. Set the radius of circle. for example = 12h
5. Set the outline color C, B and A. e.g., (0d, 0d, 40d) for red color
6. Set the filled color C, B and A. e.g., (28d, 0d, 0d) for blue color

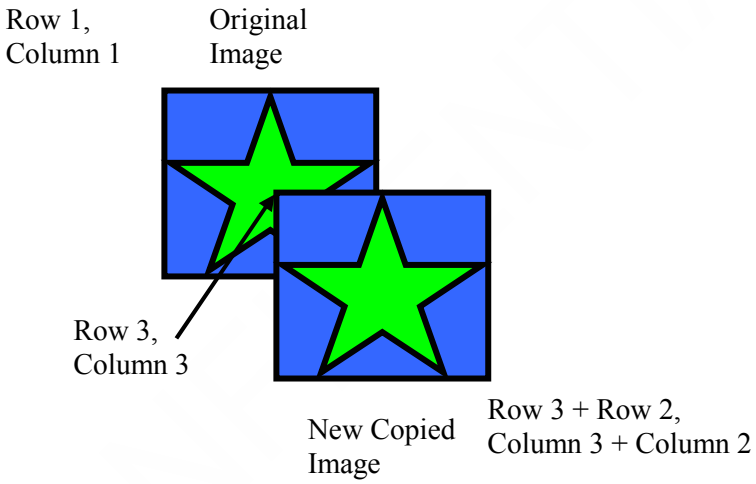
10.2.4 Copy (8Ah)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 8Ah
2. Set the starting column coordinates, Column 1. for example = 00h.
3. Set the starting row coordinates, Row 1. for example = 00h.
4. Set the finishing column coordinates, Column 2. for example = 05h
5. Set the finishing row coordinates, Row 2. for example = 05h
6. Set the new column coordinates, Column 3. for example = 03h
7. Set the new row coordinates, Row 3. for example = 03h

Figure 10-12 : Example of copy command



10.2.5 Dim Window (8Ch)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 10-1 : Result of change of brightness by dim window command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

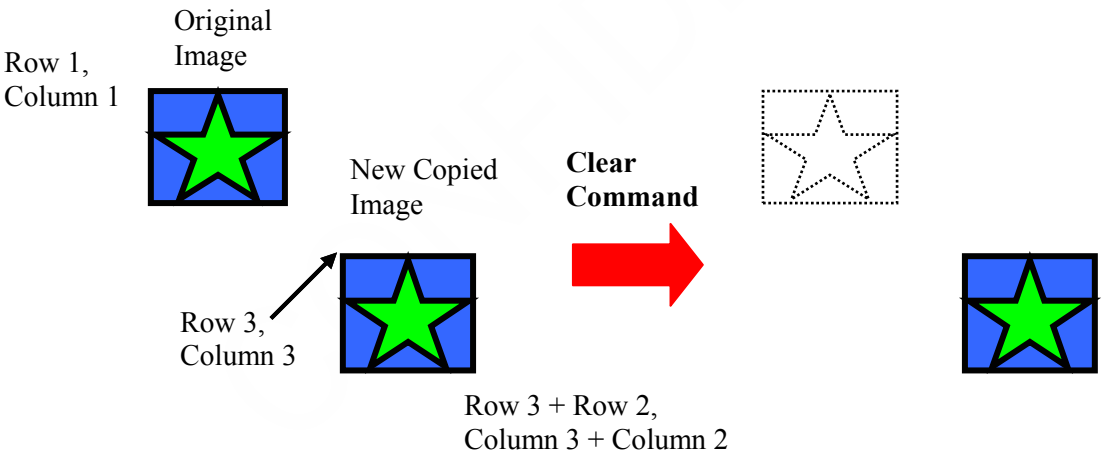
10.2.6 Clear Window (8Eh)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a "move" result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the "copy mode" by execute the command 8Ah
2. Set the starting column coordinates, Column 1. for example = 00h.
3. Set the starting row coordinates, Row 1. for example = 00h.
4. Set the finishing column coordinates, Column 2. for example = 05h
5. Set the finishing row coordinates, Row 2. for example = 05h
6. Set the new column coordinates, Column 3. for example = 06h
7. Set the new row coordinates, Row 3. for example = 06h
8. Enter the "clear mode" by execute the command 8Eh
9. Set the starting column coordinates, Column 1. for example = 00h.
10. Set the starting row coordinates, Row 1. for example = 00h.
11. Set the finishing column coordinates, Column 2. for example = 05h
12. Set the finishing row coordinates, Row 2. for example = 05h

Figure 10-13 : Example of copy + clear = Move command



10.2.7 Fill Enable/Disable (92h)

This command has two functions.

- Enable/Disable fill (A[0])
  0 = Disable filling of color into rectangle in draw rectangle command. [reset]
  1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
  0 = Disable reverse copy [reset]
  1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….

10.2.8 Horizontal Scroll (96h)

This command consists of 5 consecutive bytes to set up the horizontal scroll parameters. It determined the scrolling start page, end page and the scrolling speed.

Before issuing this command, the horizontal scroll must be deactivated (9Eh). Otherwise, RAM content may be corrupted.

10.2.9 Stop Moving (9Eh)

Stop motion of horizontal scrolling.

10.2.10 Start Moving (9Fh)

Start motion of horizontal scrolling. This command should only be issued after Horizontal scroll setup parameters are defined.

The following actions are prohibited after the horizontal scroll is activated

1. RAM access (Data write or read)
2. Changing horizontal scroll setup parameters

The SSD1339 horizontal scroll is designed for 132 columns scrolling

11 MAXIMUM RATINGS

Table 11-1 : Maximum ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{DDIO}		-0.3 to V_{DD}+0.5	V
V_{CC}		0 to 19	V
V_{REF}		0 to 19	V
V_{SEG} /V_{COM}	SEG/COM output voltage	0 to 0.9 x V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +90	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Note

(1) Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

12 DC CHARACTERISTICS

Table 12-1 : DC characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage		7	11	18	V
V_{DD}	Logic Supply Voltage		2.4	2.7	3.5	V
V_{DDIO}	Power Supply for I/O pins		1.5	2.7	V_{DD}	V
V_{OH}	High Logic Output Level	I_{OUT} =100uA, 3.3MHz	0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL}	LOW Logic Output Level	I_{OUT} =100uA, 3.3MHz	0	-	0.1*V_{DDIO}	V
V_{IH}	High Logic Input Level	-	0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL}	LOW Logic Input Level	-	0	-	0.2*V_{DDIO}	V
I_{SLEEP}	Sleep mode Current	V_{DD}=2.7V, Display OFF, No panel attached	-	-	5	uA
I_{CC}	V_{CC} Supply Current	V_{DD}=3.0V, V_{CC}=18V, Display ON Contrast =FF, No panel attached	-	1.3	-	mA
I_{DD}	V_{DD} Supply Current	V_{DD}=3.0V, V_{CC}=18V, Display ON Contrast =FF, No panel attached	-	0.4	-	mA
I_{SEG}	Segment Output Current Setting V_{DD}=2.7V, V_{CC}=11V, I_{REF}=10uA, All one pattern, Display ON, Segment pin under test is connected with a 20KΩ resistive load to V_{CC}.	Contrast = FFh	-	160	-	uA
		Contrast = AFh		110		uA
		Contrast = 5Fh	-	60	-	uA
		Contrast = 00h	-	0	-	uA
Dev	Segment output current uniformity	$Dev = (I_{SEG} - I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ where I_{SEG}[0:395] = Segment current at contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%
V_{CC}	Booster output voltage (V_{CC})	V_{IN}=3V, L=22uH; R1=450KΩ ; R2=50KΩ ; I_{CC} = 30mA(soaking)	-	12	-	V

13 AC CHARACTERISTICS

Table 13-1 : AC characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.7V	1.7	2.0	2.3	MHz
F_{FRM}	Frame Frequency for 132 MUX Mode	132RGB x 132 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1/(D*K*132)	-	Hz

Note

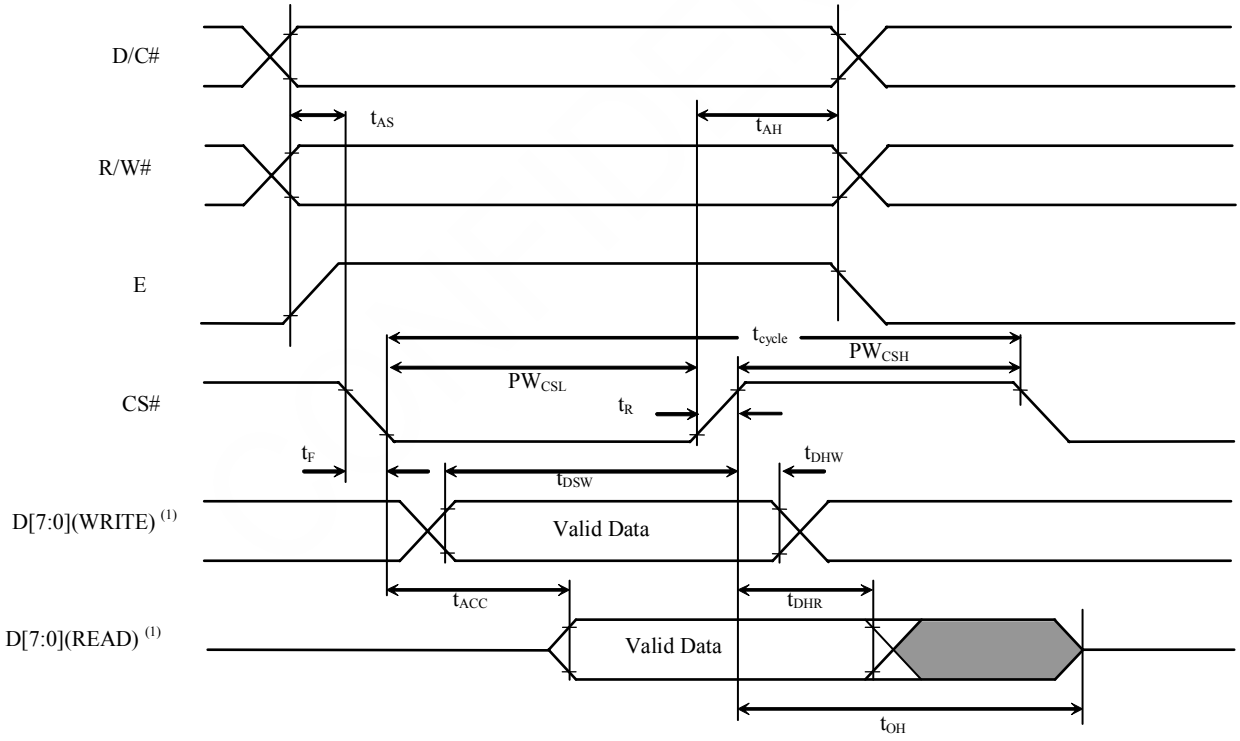
(1) D: divide ratio (reset =1)
K: number of display clocks (reset=136, i.e. phase1 DCLK+phase2 DCLK+ phase3 DCLK=4+7+125)
Refer to command table for detail description

Table 13-2 : 6800-Series MPU parallel interface timing characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select LOW Pulse Width (read) Chip Select LOW Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1 : 6800-series MPU parallel interface characteristics



Note

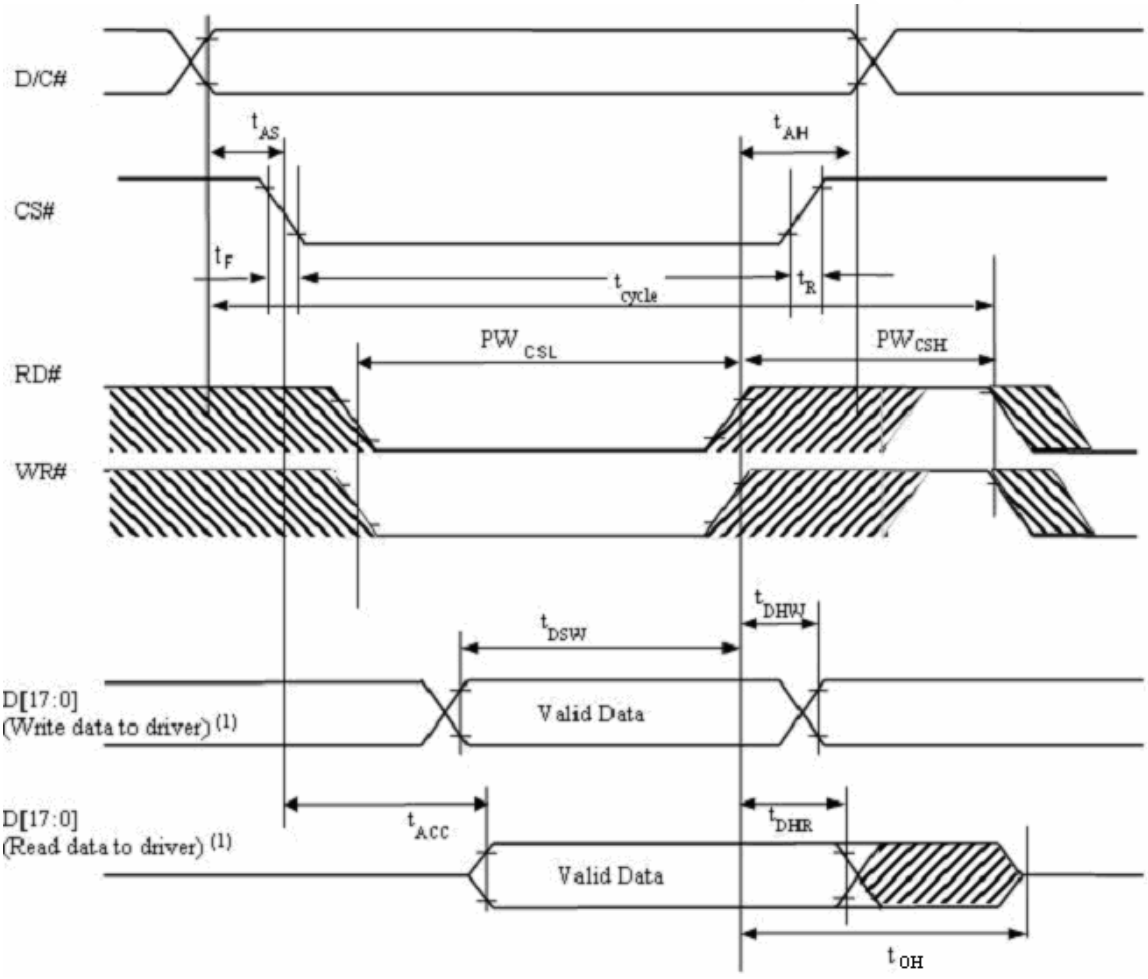
(1) When 9 bit used: D[8:0] instead; when 16 bit used: D[15:0] instead; when 18 bit used: D[17:0] instead.

Table 13-3 : 8080-Series MPU parallel interface timing characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select LOW Pulse Width (read) Chip Select LOW Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-2 : 8080-series MPU parallel interface characteristics



Note

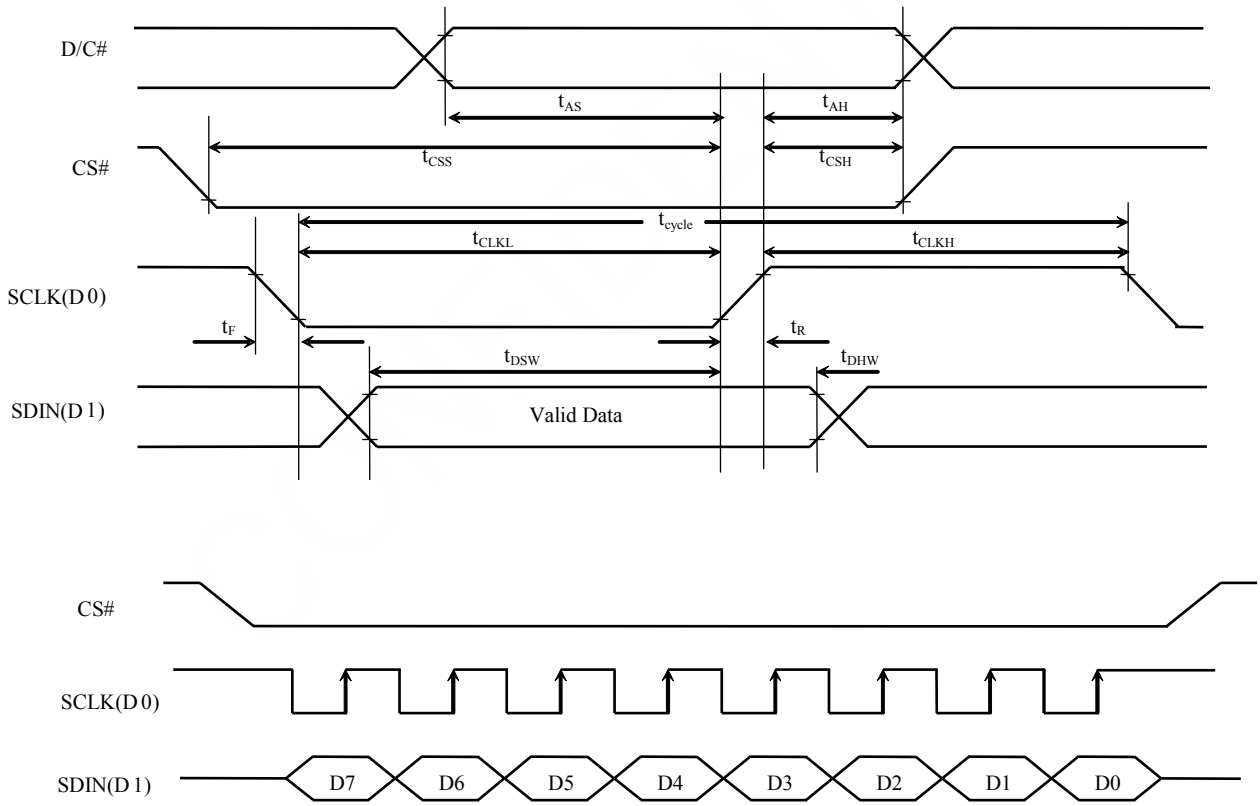
(1) When 8 bit used: D[7:0] instead; when 9 bit used: D[8:0] instead; when 16 bit used: D[15:0] instead, when 18 bit used: D[17:0] instead.

Table 13-4 : Serial interface timing characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock LOW Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

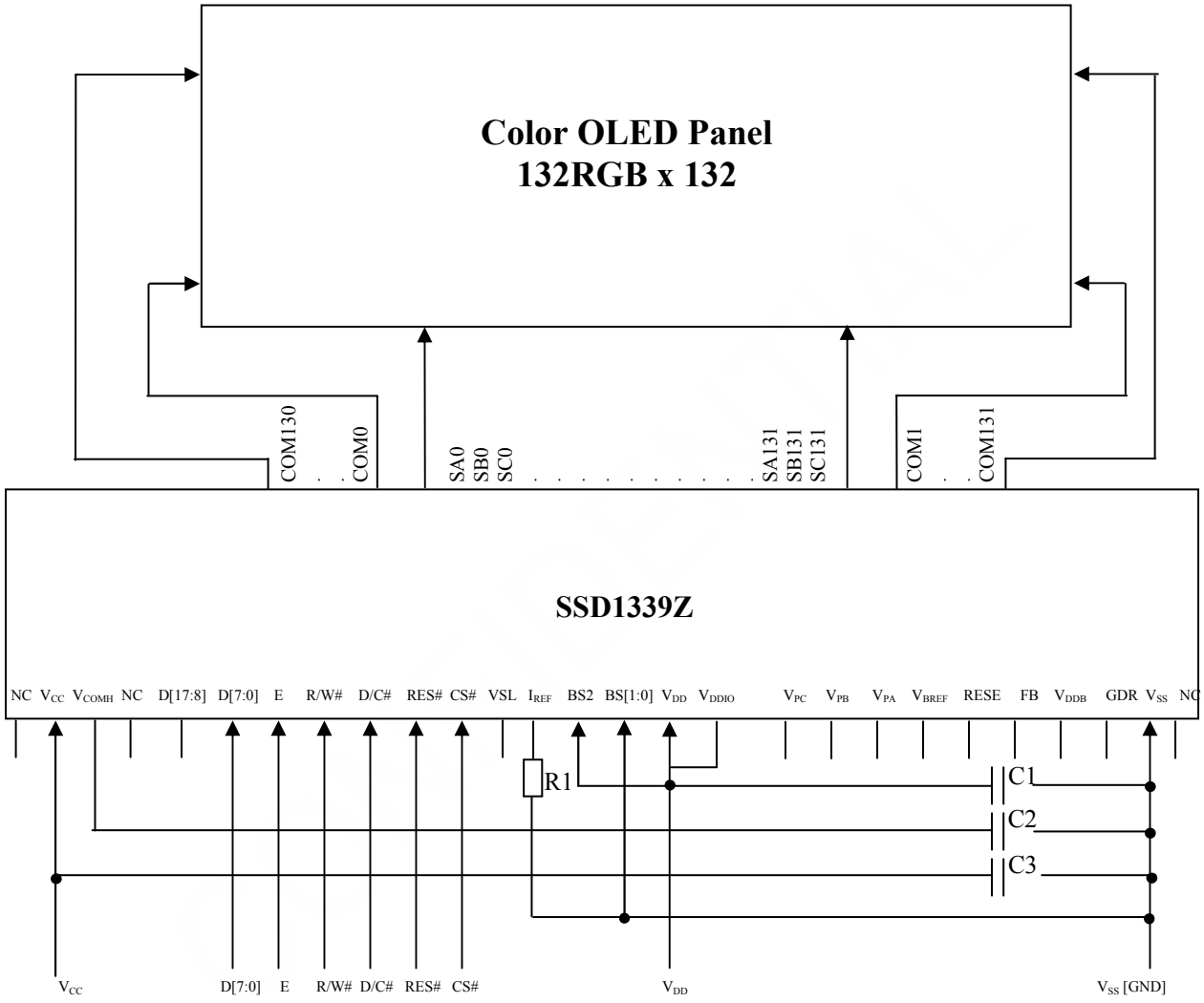
Figure 13-3 : Serial interface characteristics



14 APPLICATION EXAMPLE

Figure 14-1 : Application example for 8-bit 6800-parallel interface mode

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{DD} = V_{DDIO} = 3.0V, external V_{CC} = 12V, I_{REF} = 10uA)



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, RES#, CS#
Pin internally connected to V_{DD}: MS, CLS
Pin internally connected to V_{SS}: V_{SSB}, BGGND
Pin internally connected to V_{CC}: V_{REF}
Pin externally connected to V_{SS}: BS0, BS1
Pin externally connected to V_{DD}: BS2
Pin floated: V_{PC}, V_{PB}, V_{PA}, V_{BREF}, RESE, FB, V_{DDB}, GDR , D[17:8], VSL

C1-C3: 4.7uF [(1)]
Voltage at I_{REF} = V_{CC} – 3V
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF} = 910KΩ
Note
[(1)] The capacitor value is recommended value. Select appropriate value against module application.

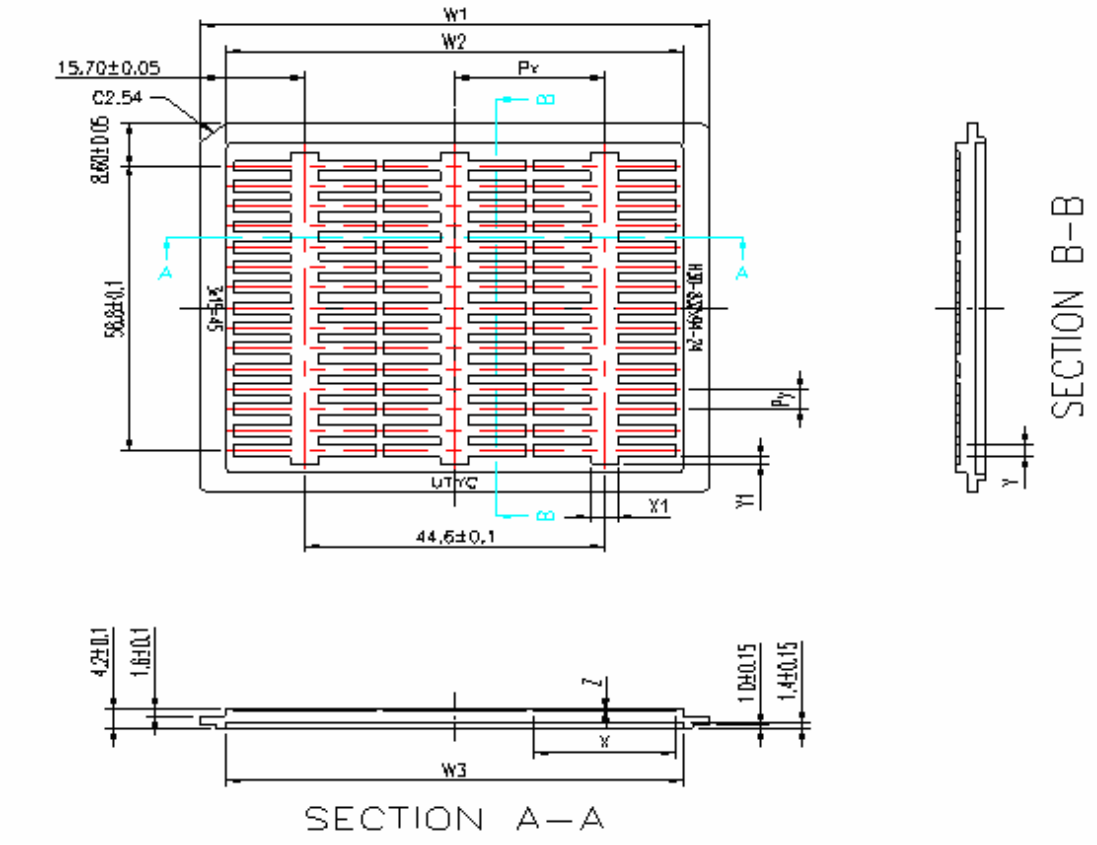
15 PACKAGE INFORMATION

15.1 SSD1339Z Die Tray Information

Figure 15-1 : Die tray information

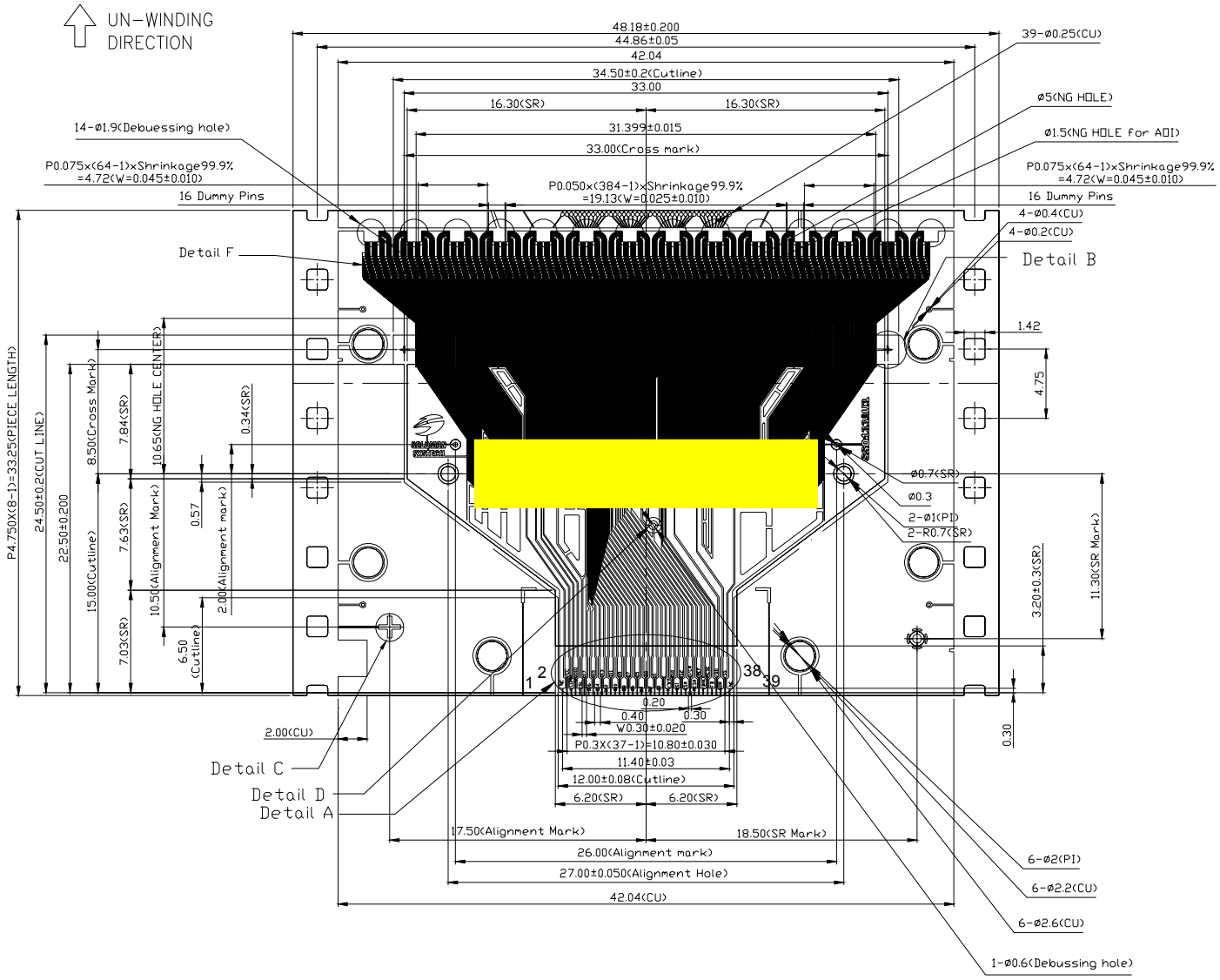
	Spec	
	mm	(mil)
W1	76.00 ± 0.1	(2992)
W2	68.00 ± 0.1	(2677)
W3	68.30 ± 0.1	(2689)
X1	4.00 ± 0.1	(157)
Y1	1.55 ± 0.1	(61)
Px	22.30 ± 0.05	(878)
Py	4.20 ± 0.1	(165)
X	21.14 ± 0.05	(832)
Y	2.40 ± 0.05	(94)
Z	0.61 ± 0.05	(24)
N	45	

Remark
1. Depth of text is 0.1mm
2. Tray material: ABS
3. Tray color code: Black
4. Surface resistance $10^9 \sim 10^{11}$ Ω - cm
5. Tray warpage: Max 0.15mm
6. Unspecifier dim's tolerance: ± 0.15mm
7. Pocket size: 21.14 x 2.40 x 0.61mm

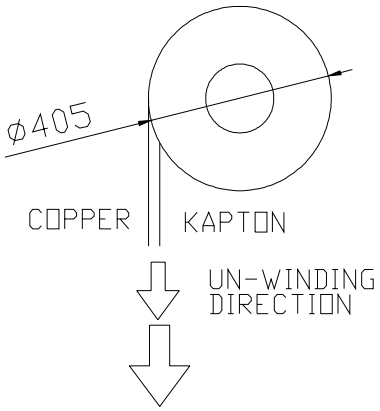


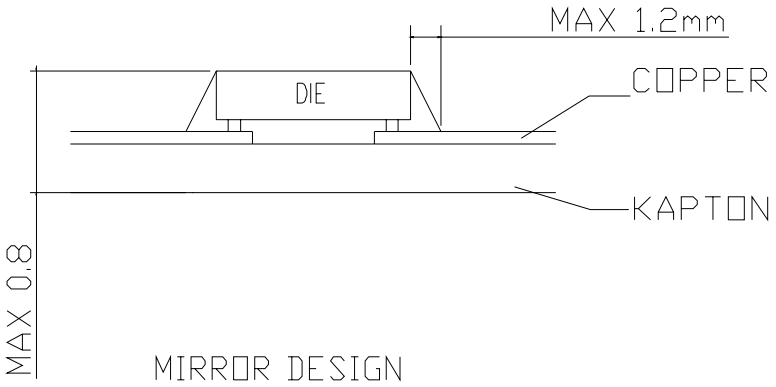
15.2 SSD1339U3R1 COF details dimensions

Figure 15-2 : SSD1339U3R1 detail dimensions

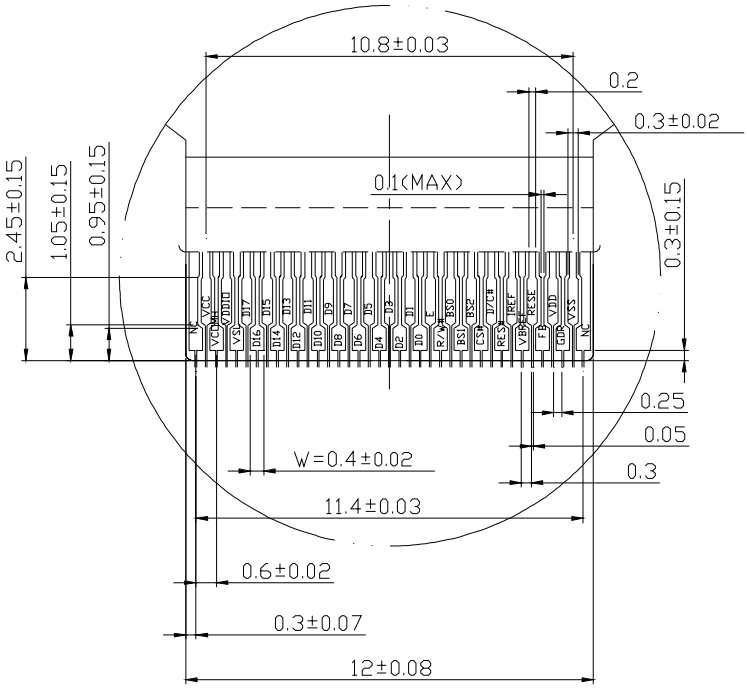


NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
   OTHER TOLERANCE: ±0.200
3. AU/Ni PLATING: AU 0.4±0.1um
   Ni 0.5±0.1um
4. TAPSITE: 7 SPH, 33.25mm



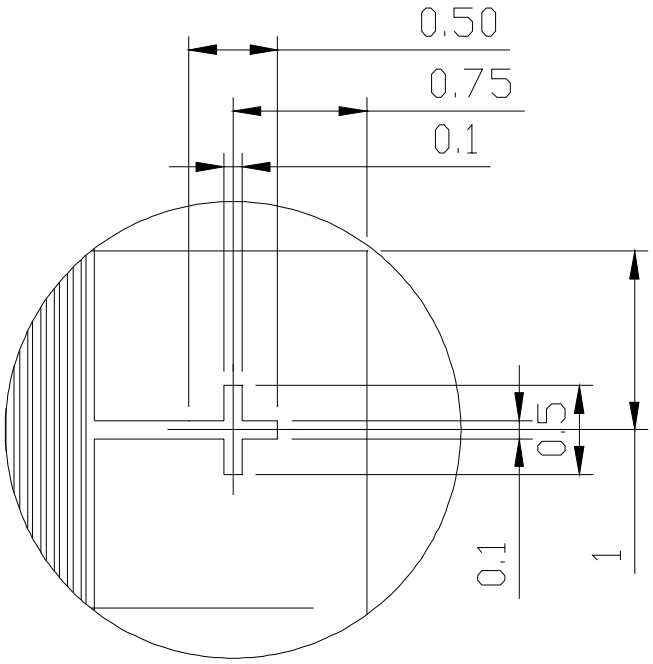


MIRROR DESIGN



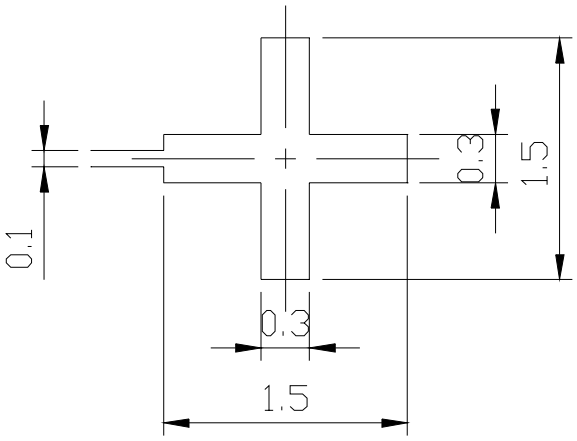
Scale: 2:1

Detail A



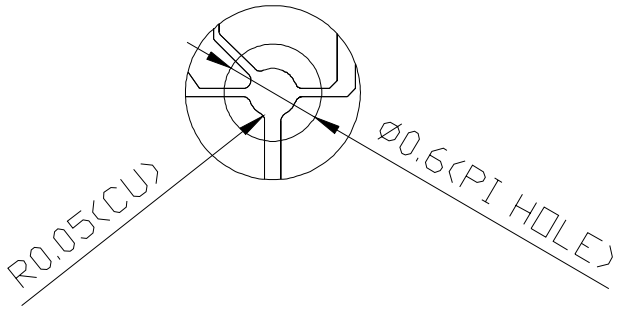
Scale: 5:1

Detail B



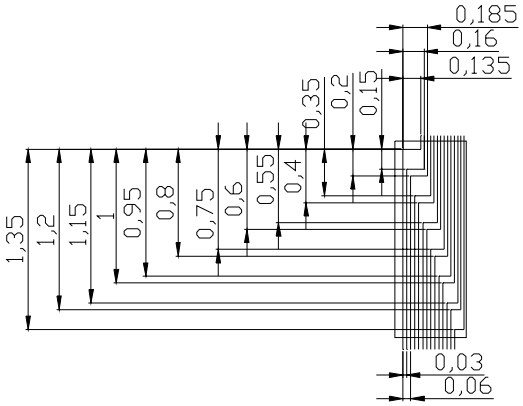
Scale: 5:1

Detail C



Scale: 5:1

Detail D

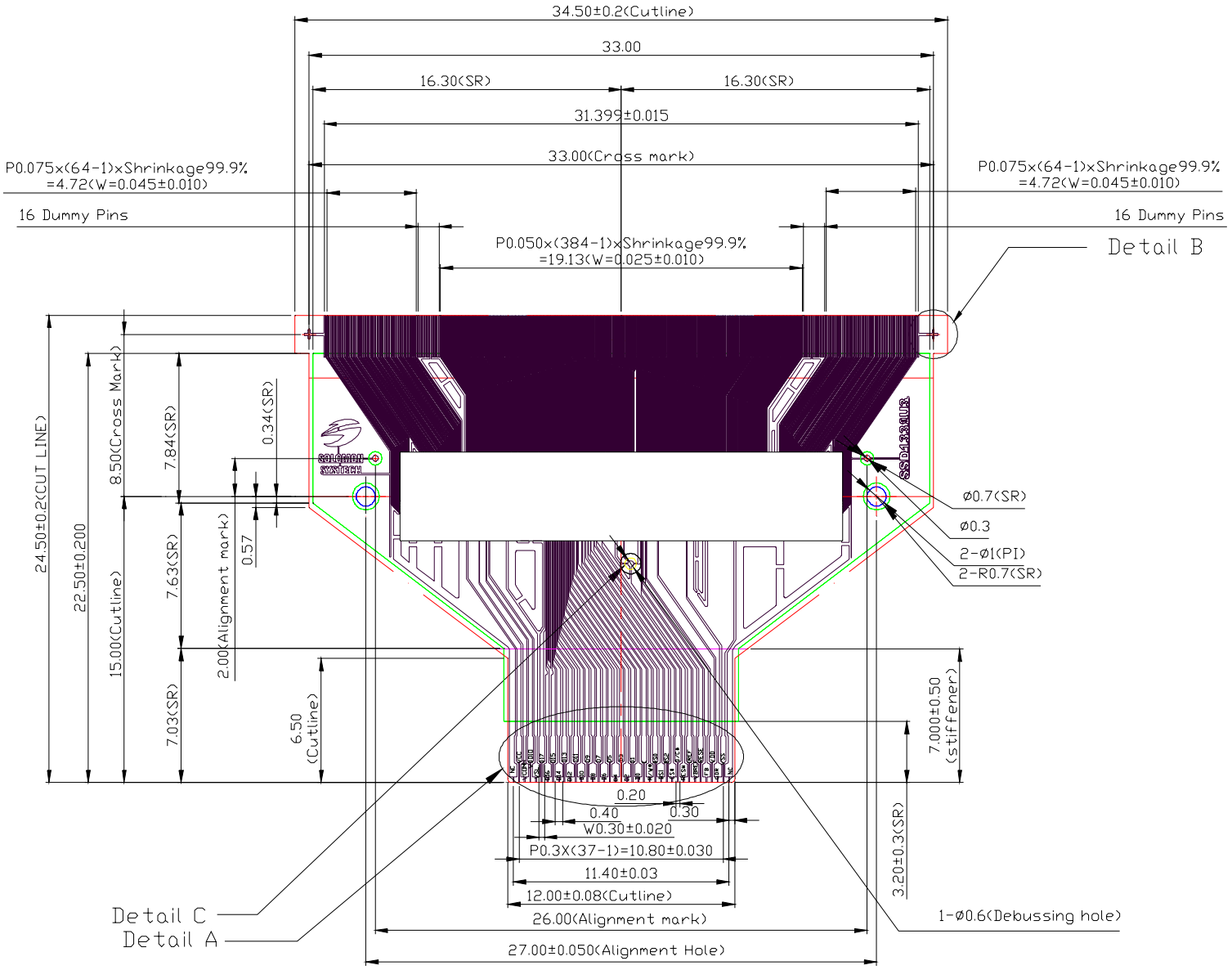


Scale: 5:1

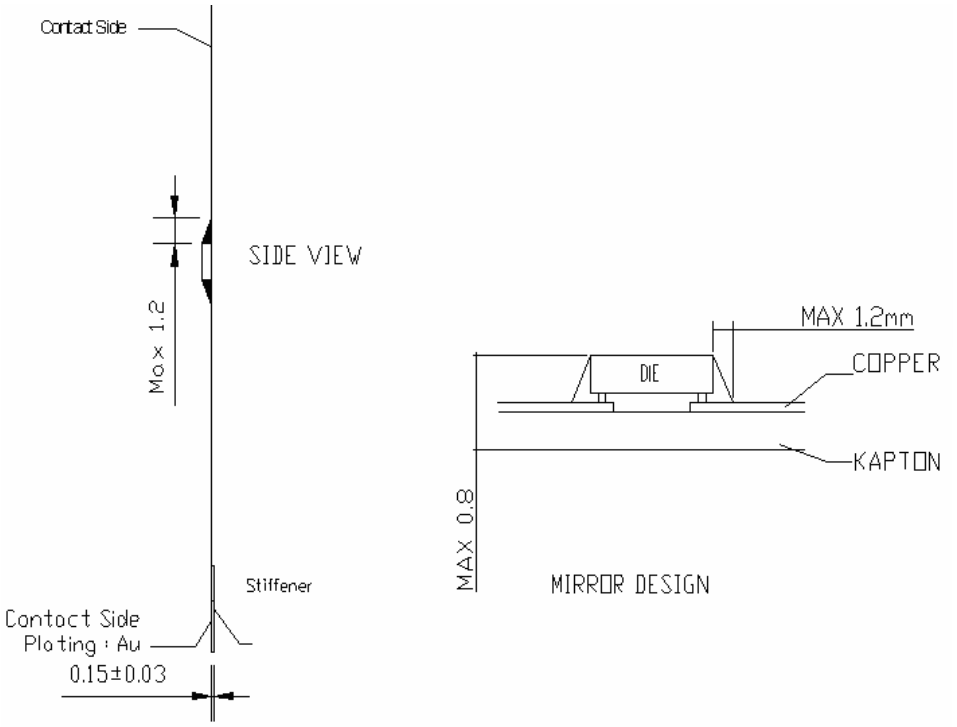
Detail F

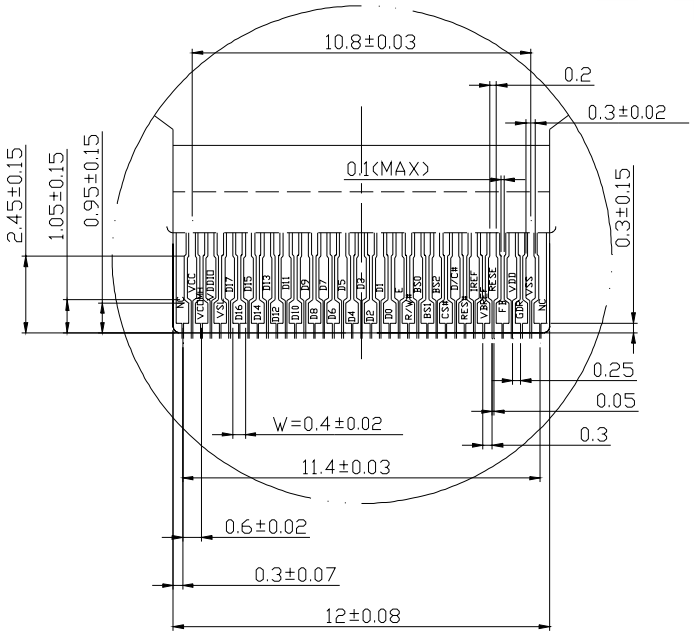
15.3 SSD1339U3 COF details dimensions

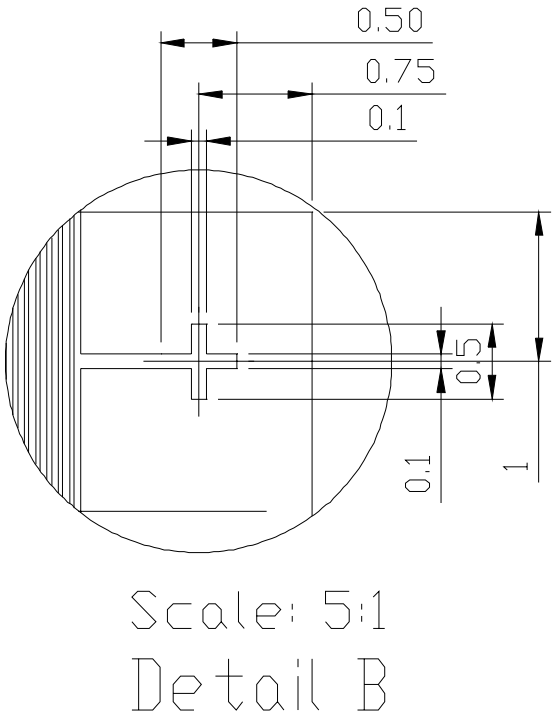
Figure 15-3 : SSD1339U3 detail dimensions



NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
   OTHER TOLERANCE: ±0.200
3. AU/Ni PLATING: AU 0.4±0.1um
   Ni 0.5±0.1um
4. TAPSITE: 7 SPH, 33.25mm


Contact Side
SIDE VIEW
Max 1.2
Stiffener
Contact Side
Plating : Au
0.15±0.03
MAX 1.2mm
COPPER
DIE
KAPTON
MAX 0.8
MIRROR DESIGN
R0.05(CU)
ø0.6(PI HOLE)
Scale: 5:1
Detail C


10.8±0.03
0.2
0.3±0.02
0.1(MAX)
2.45±0.15
1.05±0.15
0.95±0.15
0.3±0.15
0.25
0.05
0.3
W=0.4±0.02
11.4±0.03
0.6±0.02
0.3±0.07
12±0.08
Scale: 2:1
Detail A


0.50
0.75
0.1
0.5
0.1
1
Scale: 5:1
Detail B

http://www.solomon-systech.com